PI3WVR31310A, PI3WVR31313A and PI3WVR31212A in notebook and HDTV

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1.0 Introduction

The PI3WVR31XXXA switch family is developed to achieve high performance in switching high speed signals of DP1.2, DP1.3, HDMI 2.0 (PI3WVR31310A) or HDMI 1.4b (PI3WVR31313A, PI3WVR31212A) in laptop, AIO, PC, switch box, docking station, monitor and HDTV applications.

2.0 The advantage of passive MUX over active MUX in notebook design

The market appealing notebooks:

- Running for 6-8 hours in battery operation
- Boot-up after power-off for 6-8 days

Intel mobile CPU/chipset can now achieve 6W power consumption, thus:

- The ~0.4W to ~0.6W power consumption from an active MUX is high.
- Especially when compared to the <0.003W power consumption from PI3WVR31310A, which is a 99% power saving compared to an active MUX.

3.0 Why cascading of "passive MUX + active MUX" is better than "active MUX + active MUX"?

- If the 1st MUX in cascading is a passive MUX, it will consume lower power and will not generate the random jitters mostly caused by re-drivers, while the insertion loss from trace and the 1st passive MUX will be equalized by the 2nd active MUX.
- If both 1st MUX and 2nd MUX are active, the double active cascading will double power consumption and will double random jitters as well. Random jitters cannot be equalized by re-drivers thereby may fail the eye compliance test.

4.0 What is the recommended maximum DP trace for passive MUX in Intel notebook design?

In Intel Kabylake design guideline, Intel recommends maximum 8" DP1.2 trace without passive MUX and 4.1" with passive MUX as to pass DP 1.2 compliance test.
Intel deducted 3.9" trace from the 8" DP1.2 trace for the passive MUX, which is conservative for a high performance passive MUX, such as the PI3WVR3131XA family, as explained in figure 1, figure 2a, figure 2b and in table-1 below.
Based on the DP1.2 eye compliance test results of the Pericom high speed passive switch (with similar performance as equivalent to the PI3WVR313XA family) in figure 2a and figure 2b, as well the trace data in figure 1 and table-1, it is recommended as below.

Maximum 6.0" trace for DP1.2 (5.4Gbps) path, as:

- Intel DP1.2 source → PI3WVR3131XA → DP connector

Maximum 3.5" trace for DP 1.3 (8Gbps) path, as:

- Intel DP1.3 source → PI3WVR3131XA → DP connector

(Assuming the layout and schematics are as recommended as using 90ohm traces without chokes, etc., and in reasonable system conditions)

Table 1 the insertion loss of Pericom high speed passive MUX (equivalent to PI3WVR3131XA) versus Intel trace board

	Insertion loss of 3" trace on Intel trace board	Per inch	Pericom high speed passive switch (equivalent to PI3WVR31313A)		
			Insertion loss	Equivalent trace length (loss of switch/ loss of 1" trace)	Good-maximum DP1.2 trace in Intel 8" trace topology
Insertion loss at 5.4Gbps (DP1.2)	-2.3db	-0.77db	-1.5db	1.95" (1.5db/0.77db)	6.05" (8"-1.95")

Table 1 the insertion loss of the 3" FR4 differential trace was measured using Intel trace board and Agilent N5230A 20GHz Network Analyzer, as setup in figure-1.

4.1 The insertion loss of 3” differential trace on Intel trace board

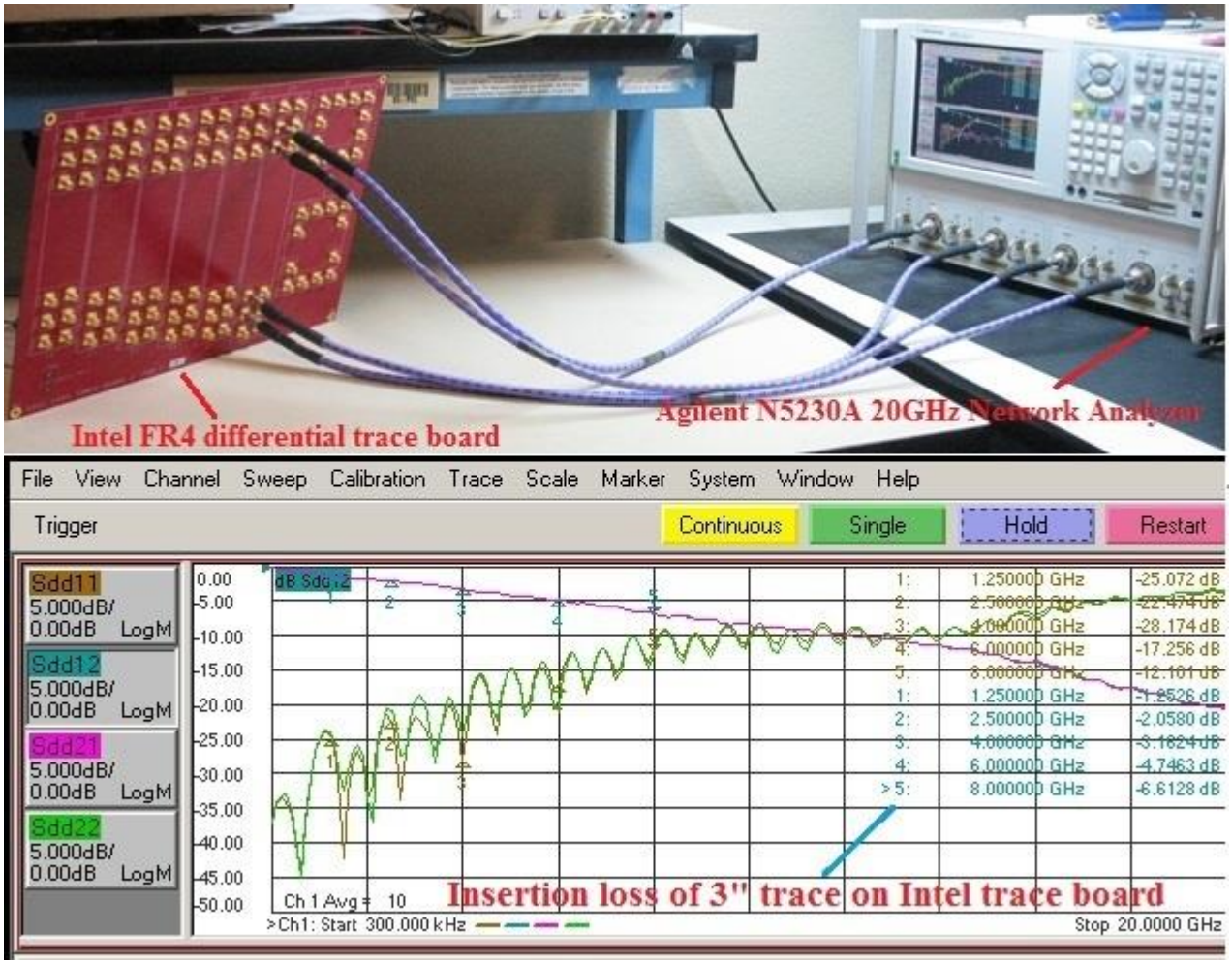


Figure 1 the insertion loss of 3” FR4 differential trace on Intel trace board is measured using Agilent N5230A 20GHz Network Analyzer (chart by James Liu)

4.2 The Pericom high speed switch (with similar performance as equivalent to PI3WVR3XXXA) and Intel Haswell MB DP1.2 eye compliance test result

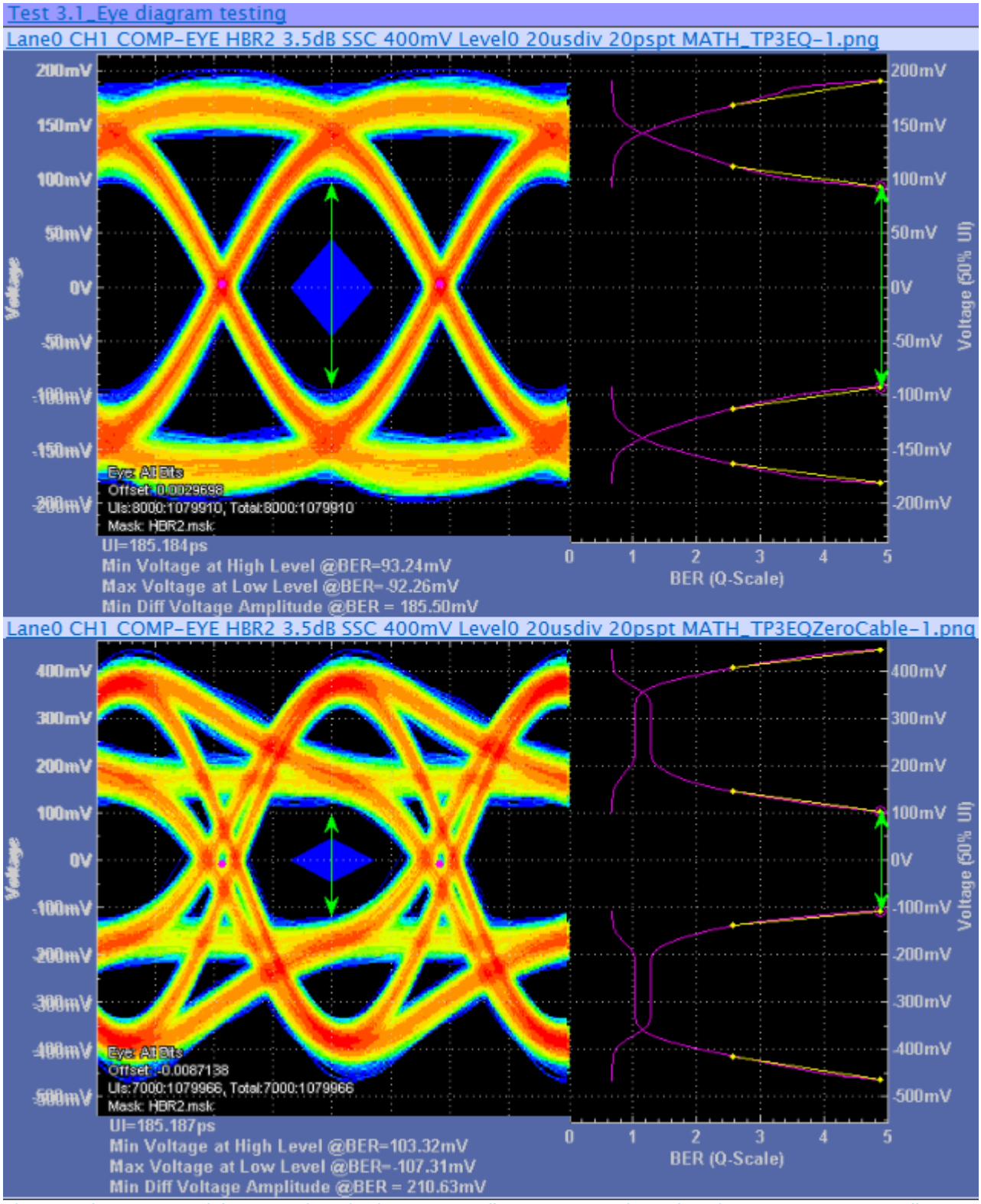


Figure 2a the eye passed the DP1.2 (5.4Gbps) HBR2 compliance test 3.1 using Tektronix scope at 400mV, 3.5db pre-emphasis. The upper waveform is at T3 with emulation cable in scope. The lower waveform is at T2 without emulation cable (waveform by Jerry Chou). See test setup in figure 2b using Pericom high speed switch equivalent to PI3WVR31XXXA, with Asus H97i Intel Haswell MB and 7" DP trace.

4.3 The test setup of 4.2

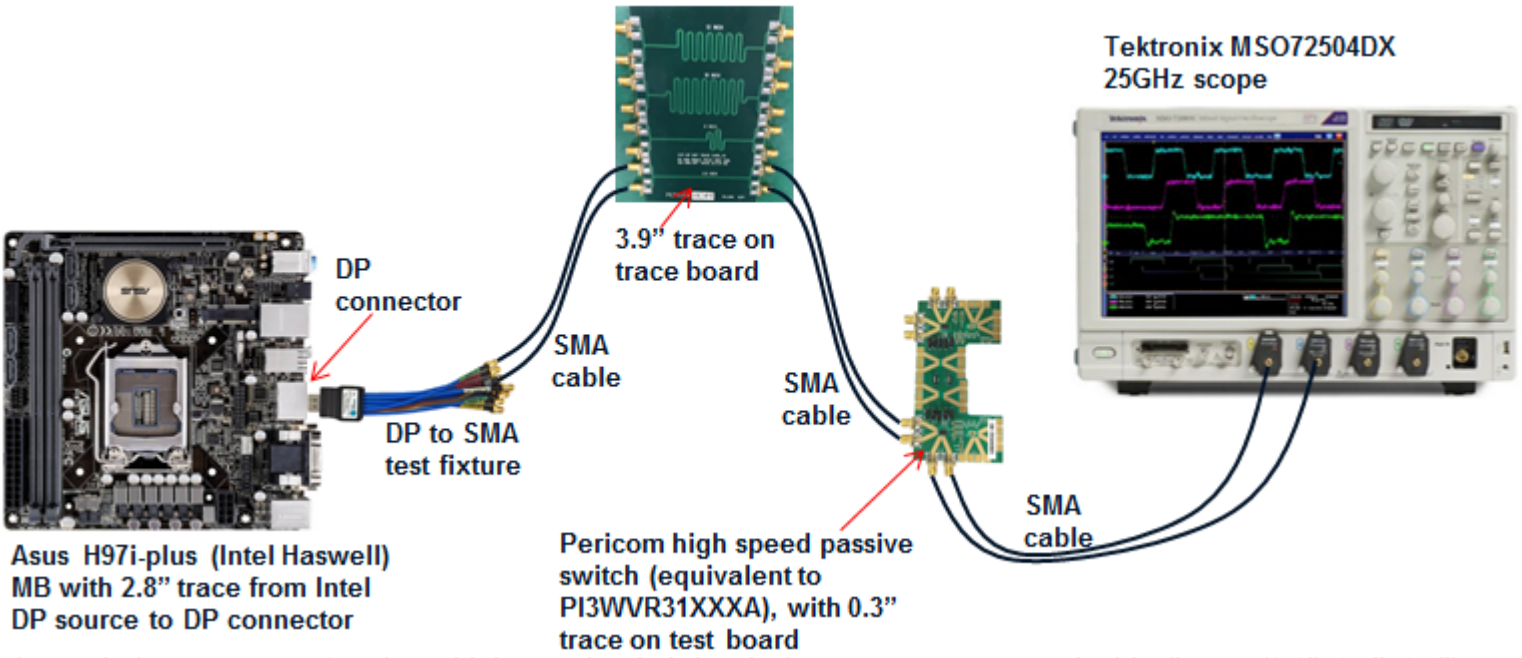


Figure 2b the test setup of Pericom high speed switch (equivalent to PI3WVR31XXXA) with 7" trace (2.8"+3.9"+0.3") using Intel Haswell DP1.2 source has passed DP1.2 (5.4Gbps) eye compliance test 3.1 as in figure 2a

5.0 PI3WVR31XXXA function selection table

PI3WVR31313A/31310A/31212A function selection table-2a

	Output ports	Pin control	I2C control	ESD	Package
PI3WVR31313A	2 passive DP ports 1 active HDMI port	Auto (no manual) HPD priority, 3-EQ settings, 3 PRE_EM settings	HDMI Port 3: 8-EQ, 5 PRE_EM, all settings, more…	Port 1-2: 2KV/HBM Port 3: 8KV/contact	60 pin TQFN package (5x9mm, 0.4mm pitch)
PI3WVR31310A	3 passive DP/HDMI ports	Priority settings, DP-HDMI selections, more…	No I2C control	Port 1-2-3: 2KV/HBM	60 pin TQFN package (5x9mm, 0.4mm pitch)
PI3WVR31212A	1 passive DP port 1 active HDMI port	Auto (no manual) HPD priority, 3-EQ settings, 3 PRE_EM settings	HDMI port 2: 8-EQ, 5 PRE_EM, all settings, more…	Port 1: 2KV/HBM Port 2: 8KV/contact	60 pin TQFN package (5x9mm, 0.4mm pitch)

PI3WVR31313A/31310A/31212A function selection table-2b

	Shutdown	DP-channel Operation power	HDMI-channel Operation power	DP Insertion loss/5.4Gbps	HDMI active output trace (with reasonable layout-topology)
PI3WVR31313A	70uA	0.002mW (615uAx3.3V)	264mW (80mA x 3.3V)	1.5db	4"-6"
PI3WVR31310A	70uA	0.002mW (615uAx3.3V)	70uA	1.5db	NC
PI3WVR31212A	70uA	0.002mW (615uAx3.3V)	264mW (80mA x 3.3V)	1.5db	4"-6"

6.0 PI3WVR31XXXA in Notebook PC, DP monitor and HDTV applications

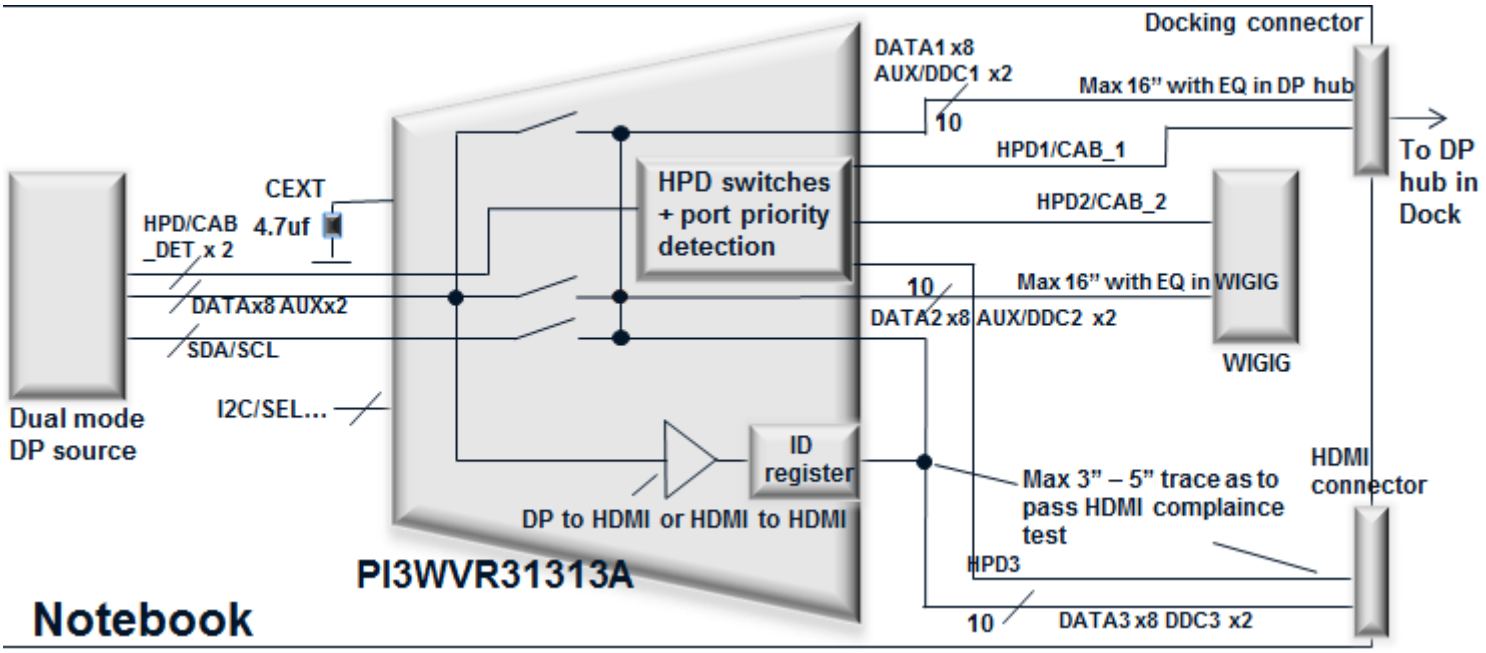


Figure 3, PI3WVR31313A in notebook with docking connector, HDMI connector and WIGIG

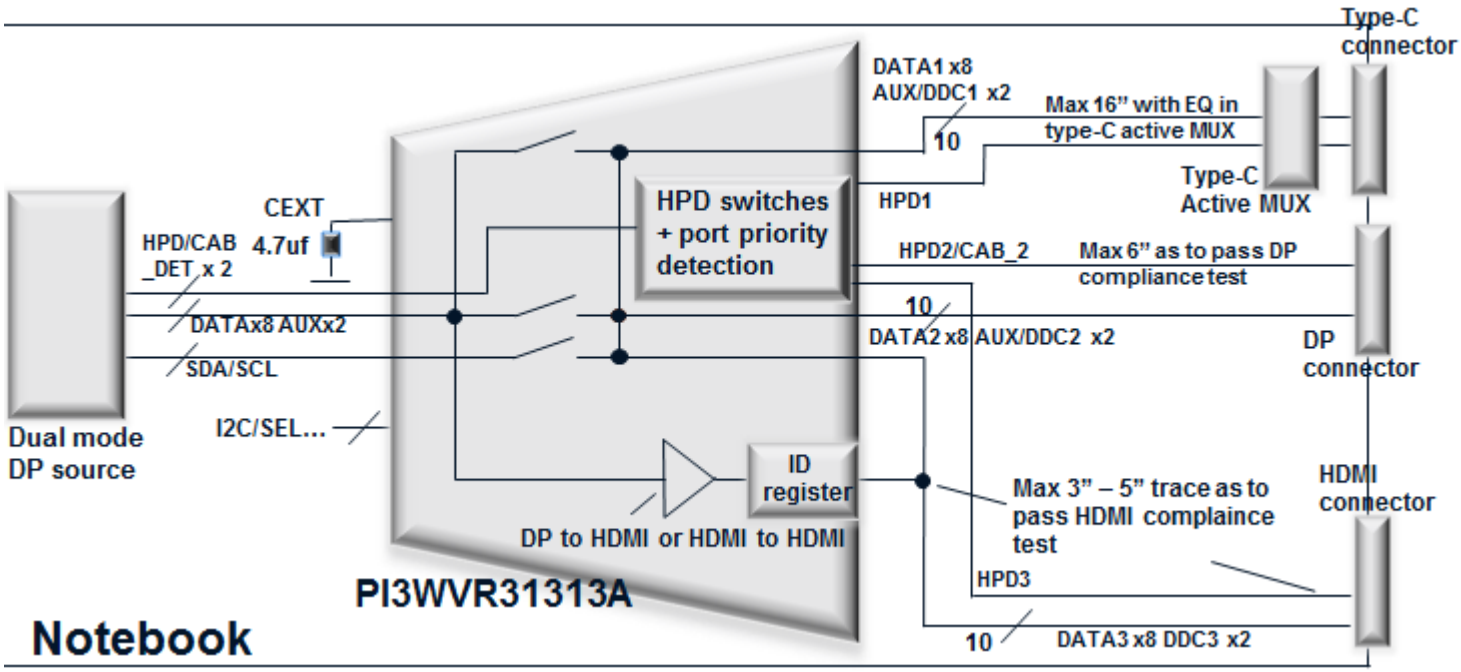


Figure 4, PI3WVR31313A in notebook with type-C connector, DP connector and HDMI connector

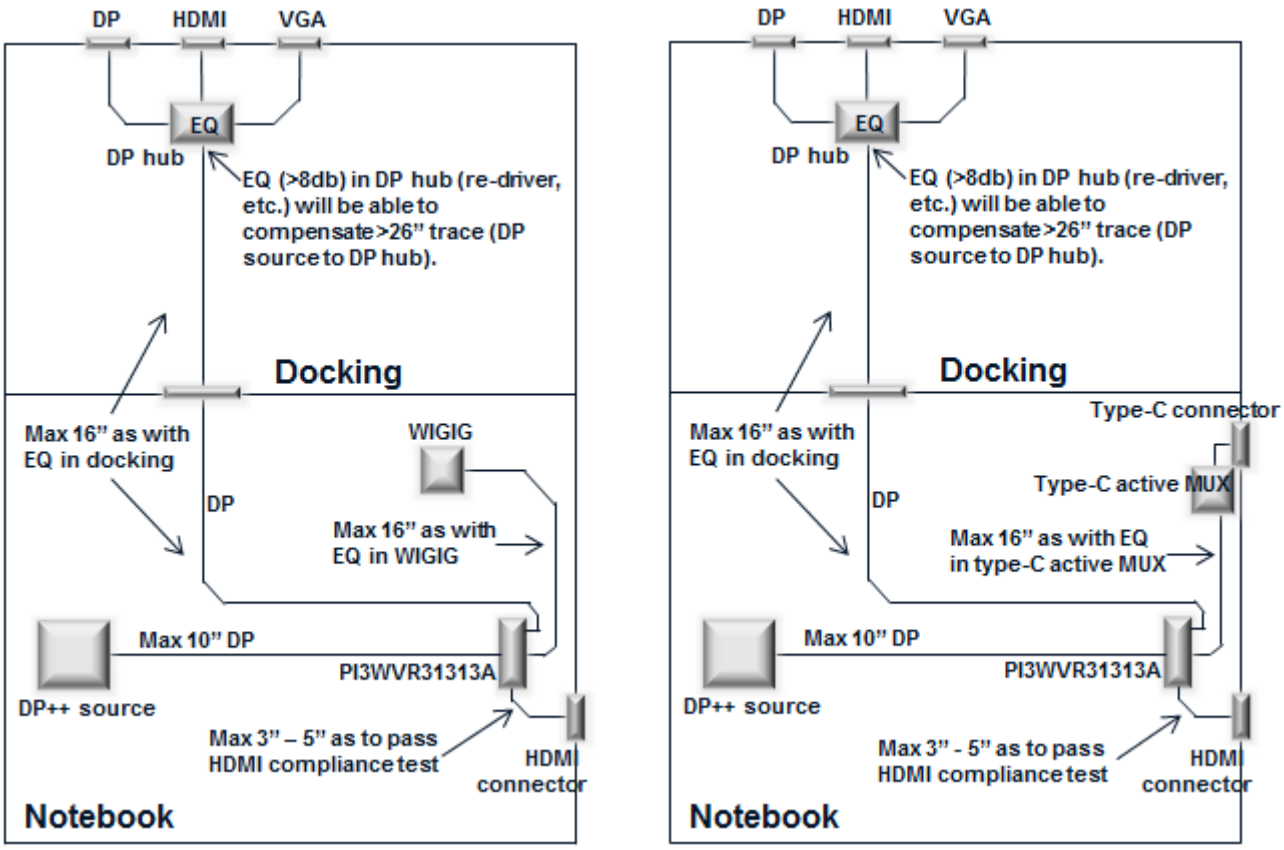


Figure 5, PI3WVR31313A in notebook with type-C connector, DP connector and HDMI connector

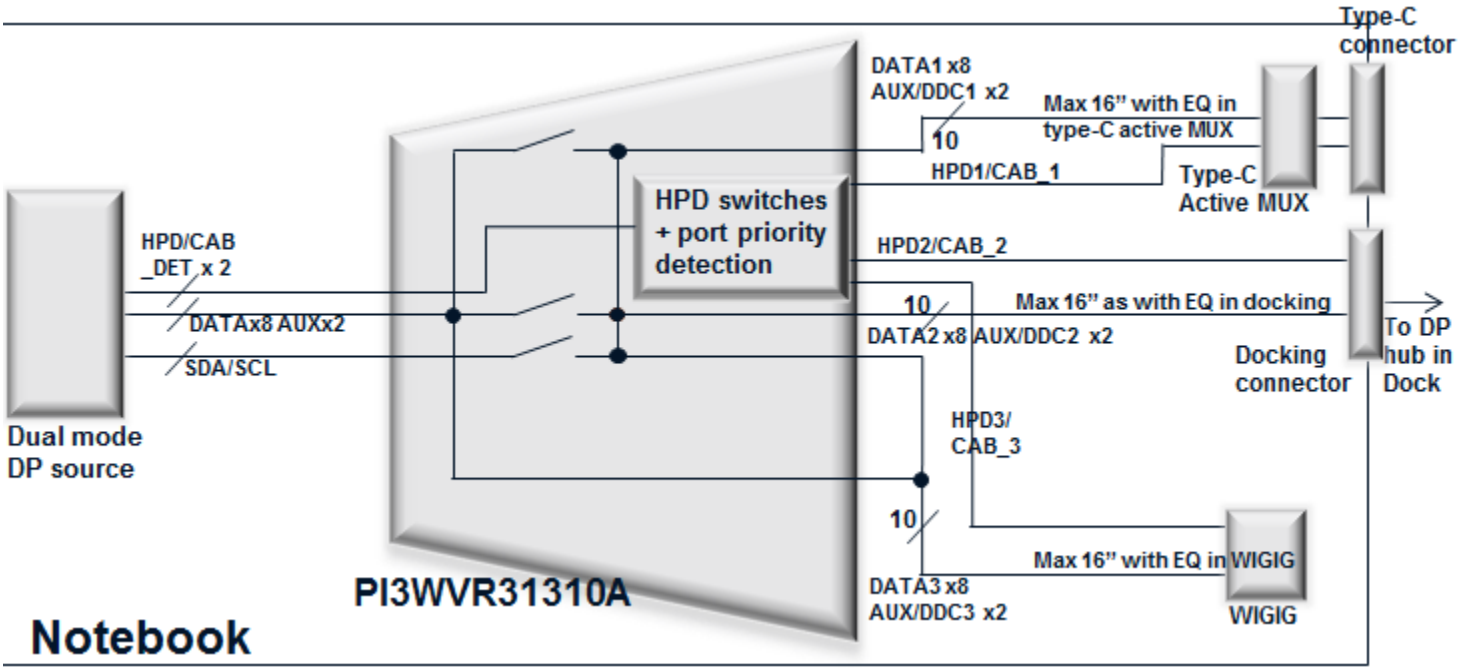


Figure 6, PI3WVR31310A in notebook with type-C connector, docking connector and WIGIG

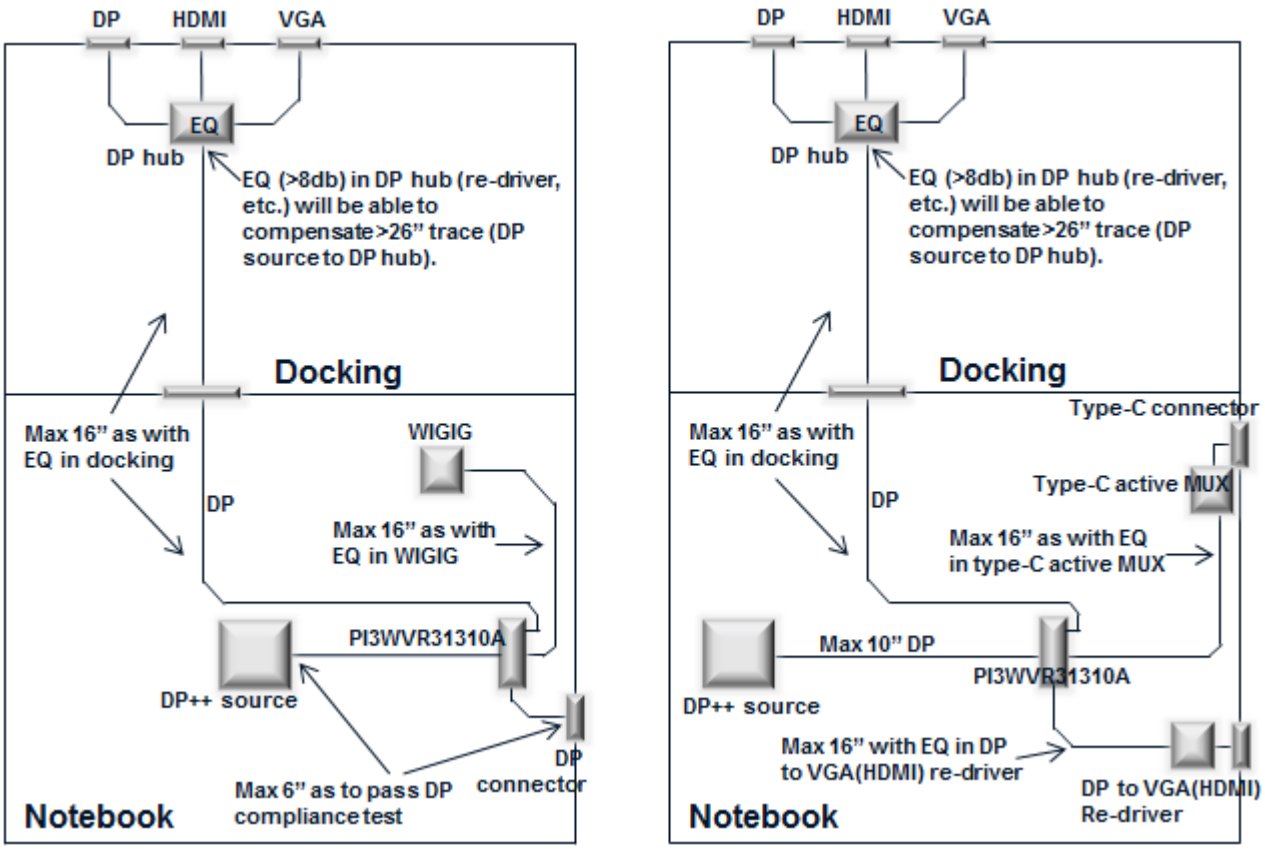


Figure 7, PI3WVR31310A in notebook with type-C connector, DP connector and HDMI connector

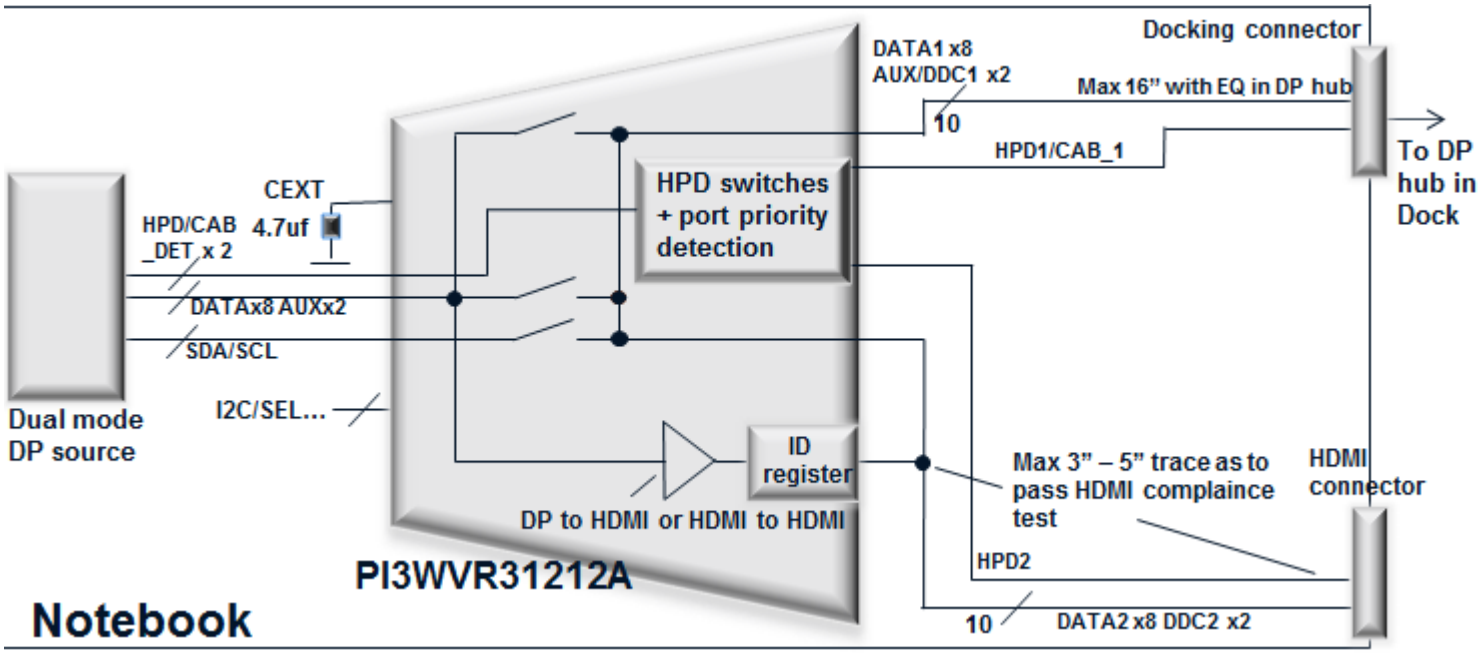


Figure 8, PI3WVR31212A in notebook with docking connector and HDMI connector

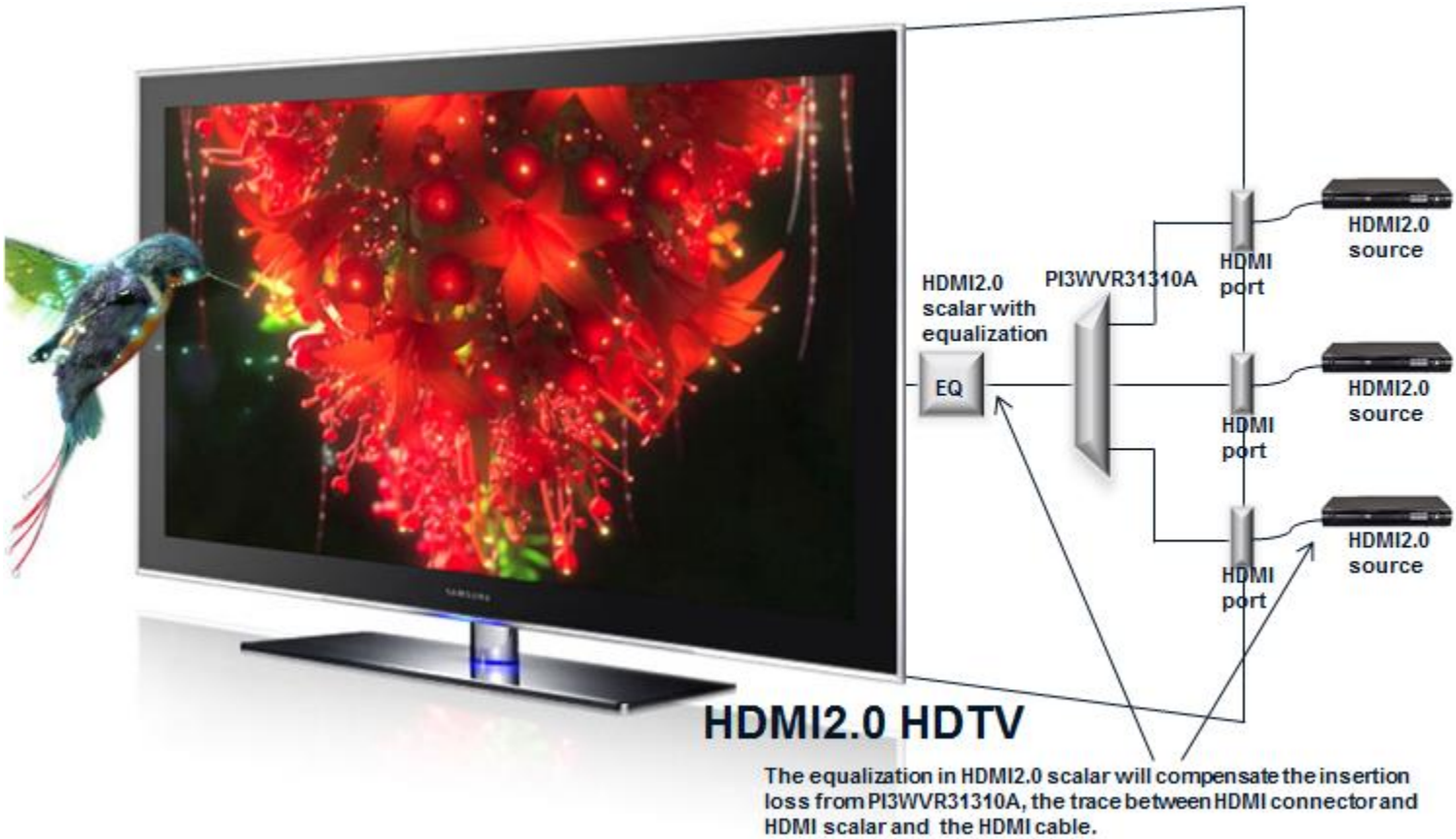


Figure 9, PI3WVR31310A in HDMI 2.0 HDTV

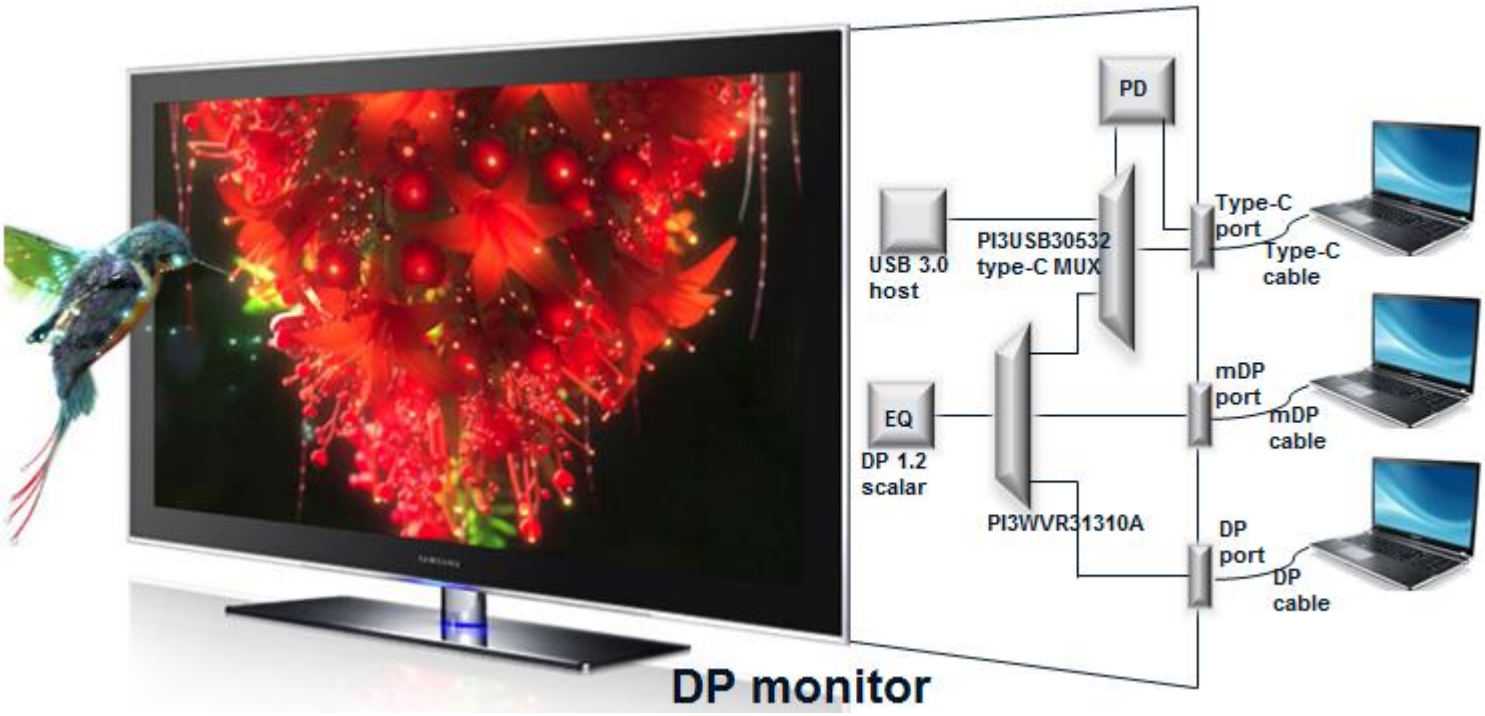


Figure 10, PI3WVR31310A and PI3USB30532 in type-C DP monitor

- No active DP re-driver needed in type-C MUX (PI3USB30532) or between PI3USB30532 and PI3WVR31310A in cascading.
  - Because there are sufficient total source and sink equalization, as:
    - Up to 9db output pre-emphasis (equalization) in DP source
    - Up to 9db input equalization in DP sink scalar
  - The total 18db equalization in DP source and DP sink is sufficient to compensate the estimated total insertion loss from the topology in figure 10:
    - Max 7.7db from total 10" traces
    - Max 4db from 2 meter type-Cable
    - Max 1.5db from PI3USB30532
    - Max 1.5db from PI3WVR31310A

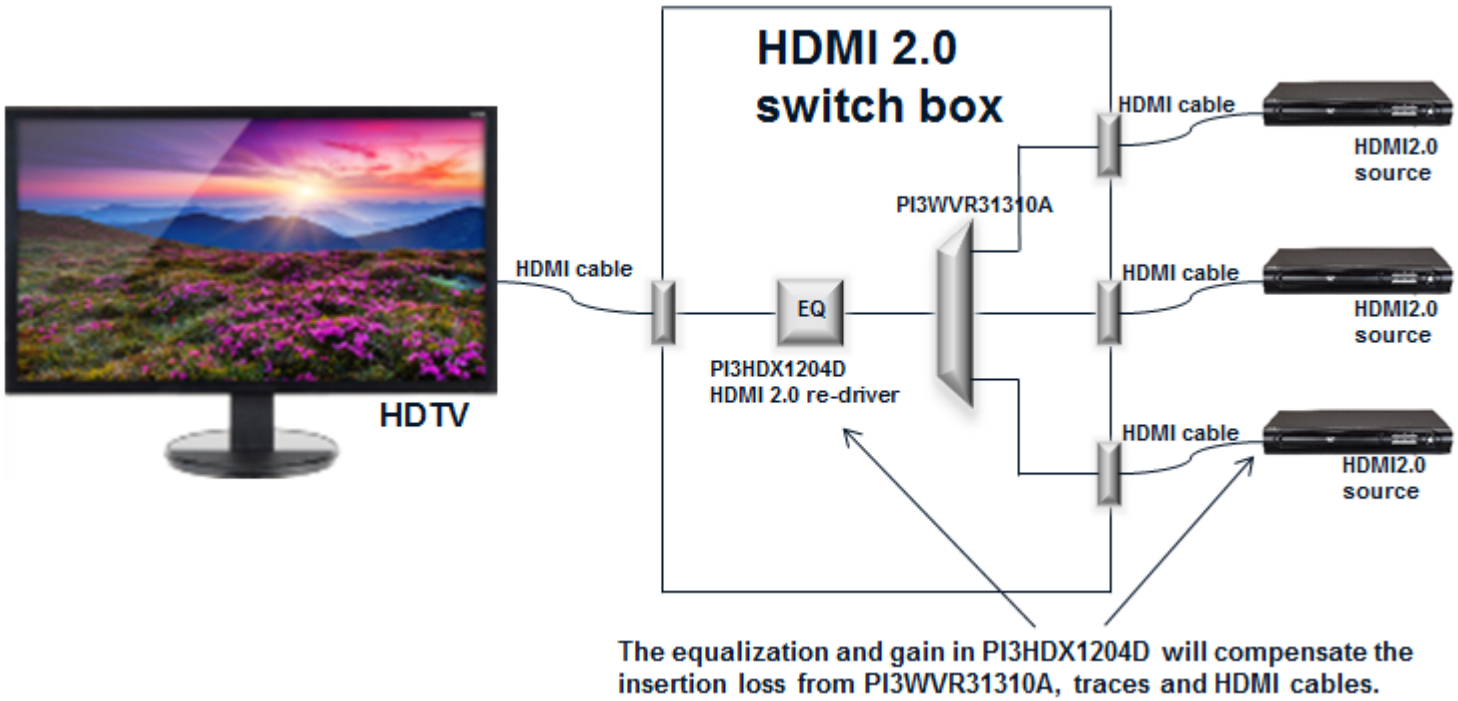
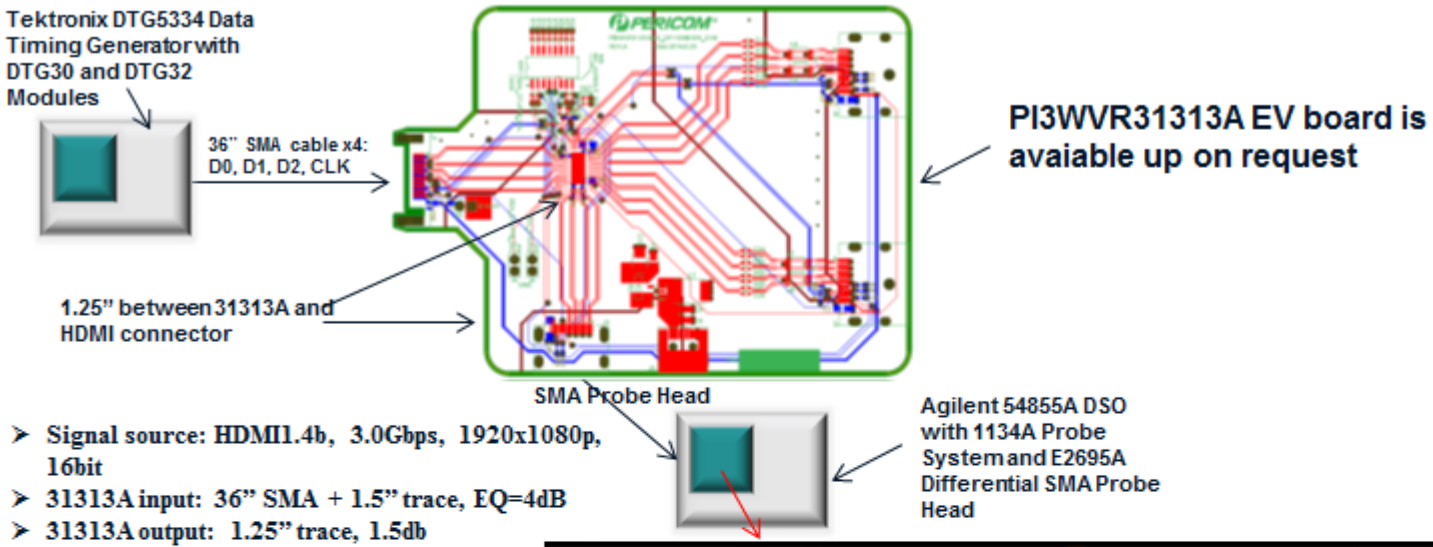


Figure 11, PI3WVR31310A in HDMI 2.0 switch box

7.0 PI3WVR31313A HDMI 1.4b eye compliance test and DP re-driver equalized long trace 6.0Gbps eye test

HDMI1.4b compliance test result of the HDMI channel in PI3WVR31313A



- **Signal source: HDMI1.4b, 3.0Gbps, 1920x1080p, 16bit**
- **31313A input: 36" SMA + 1.5" trace, EQ=4dB**
- **31313A output: 1.25" trace, 1.5db pre-emphasis, 500mV swing**

Test ID	Pass/Fail	Value
7-4: TMDS – TRISE, TFALL	Pass	TRISE CK: 106.41ps D0: 99.56ps TFALL CK: 121.04ps D0: 108.10ps
7-8: TMDS – Clock Duty Cycle	Pass	Clock Duty: Min = 48.87 % Max = 50.14 %
7-9: TMDS – Clock Jitter	Pass	Clock Jitter 114 mTbit
7-10: TMDS – data Eye Diagram (see the eye on the right)	Pass	D Jitter 186 mTbit

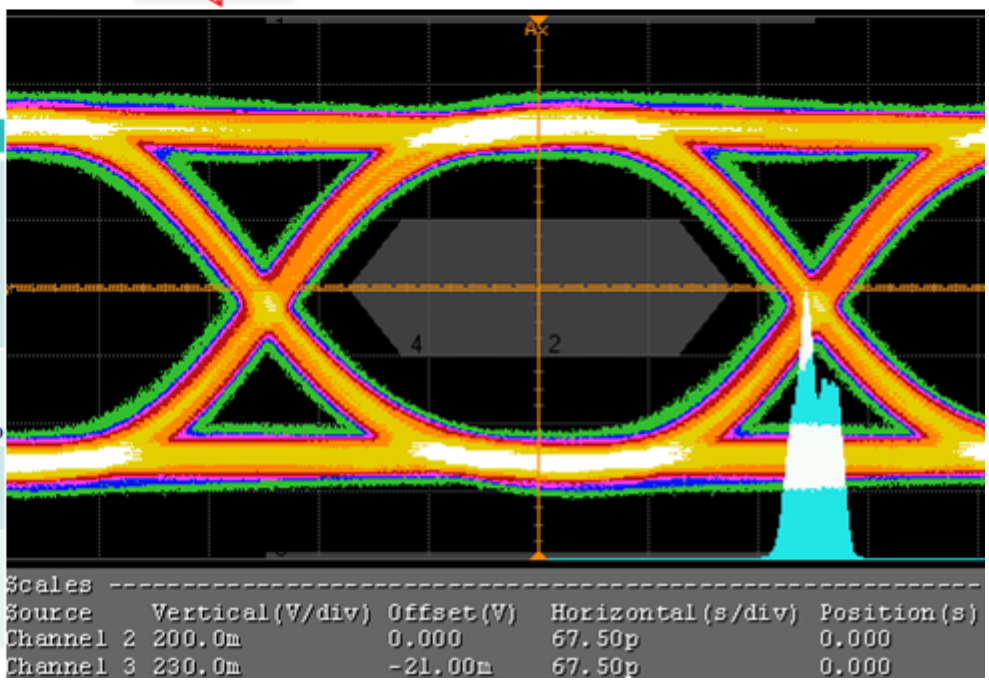


Figure 12, PI3WVR31313A passed HDMI 1.4b eye compliance test (waveform by Ada Yip)

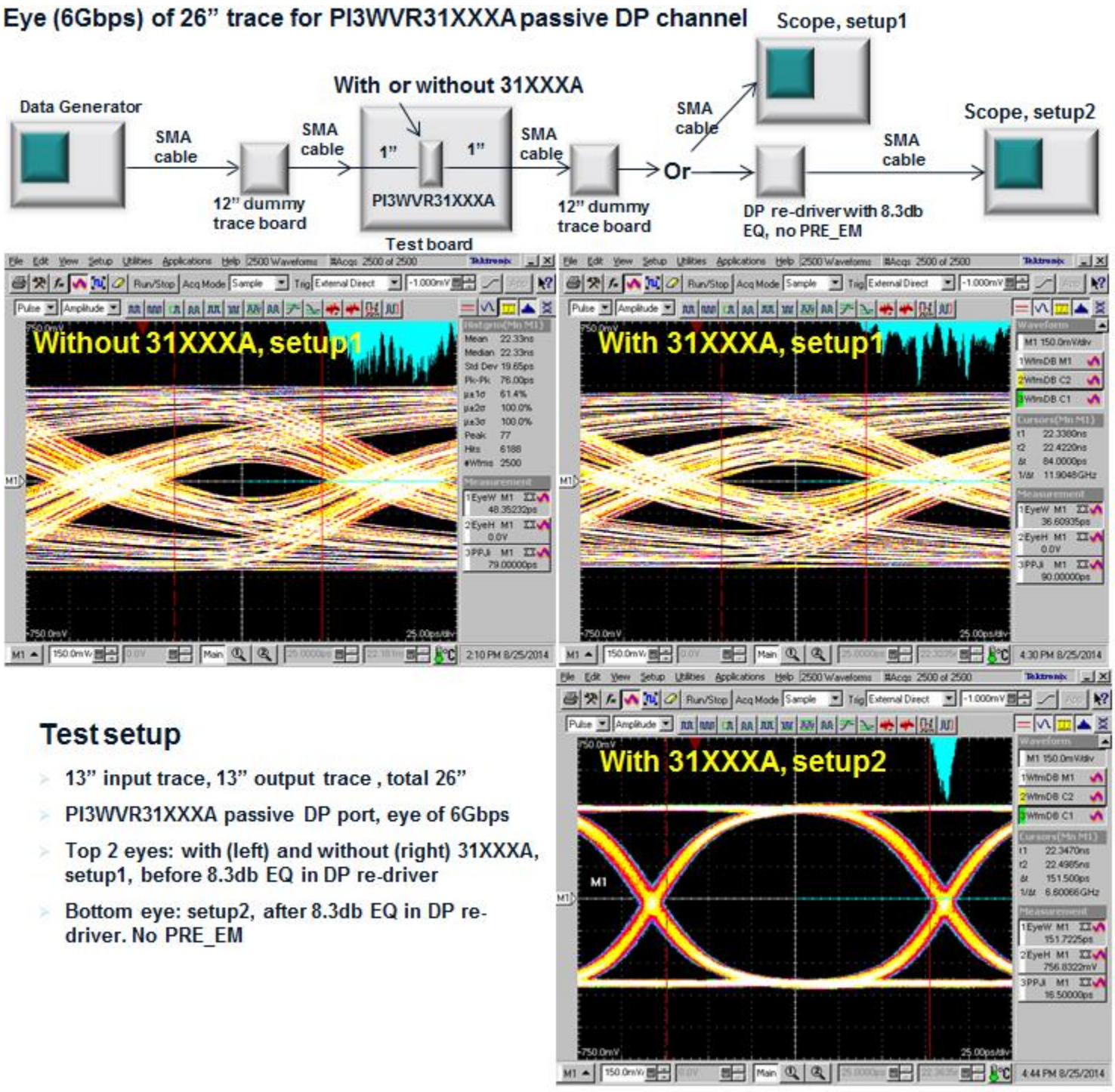


Figure 13, the 8.3db equalization in DP re-driver has well compensated the insertion loss from PI3WVR31XXXA and 26" trace (waveform by Nikolay Vitchev)

8.0 Recommendation of system timing

- When laptop is power-on at T0 (figure-14), laptop will take 2s - 20s uploading Windows, then, Windows will start to detect HPD-high at HPD_SRC, at T2.
- When laptop powers-on at T0 and sequentially powers-on the VDD of PI3WVR3131XA at T1, PI3WVR3131XA will take ~0.8s to detect the HPD-high at the 3 DP output port1, port2, port3 of PI3WVR3131XA and then inform the DP source and Windows thru HPD_SRC.
- In order for Windows to correctly detect HPD-high at the 3 DP outputs ports in-time, system EC (MCU) shall control T1 to be >2.0s earlier than T2.

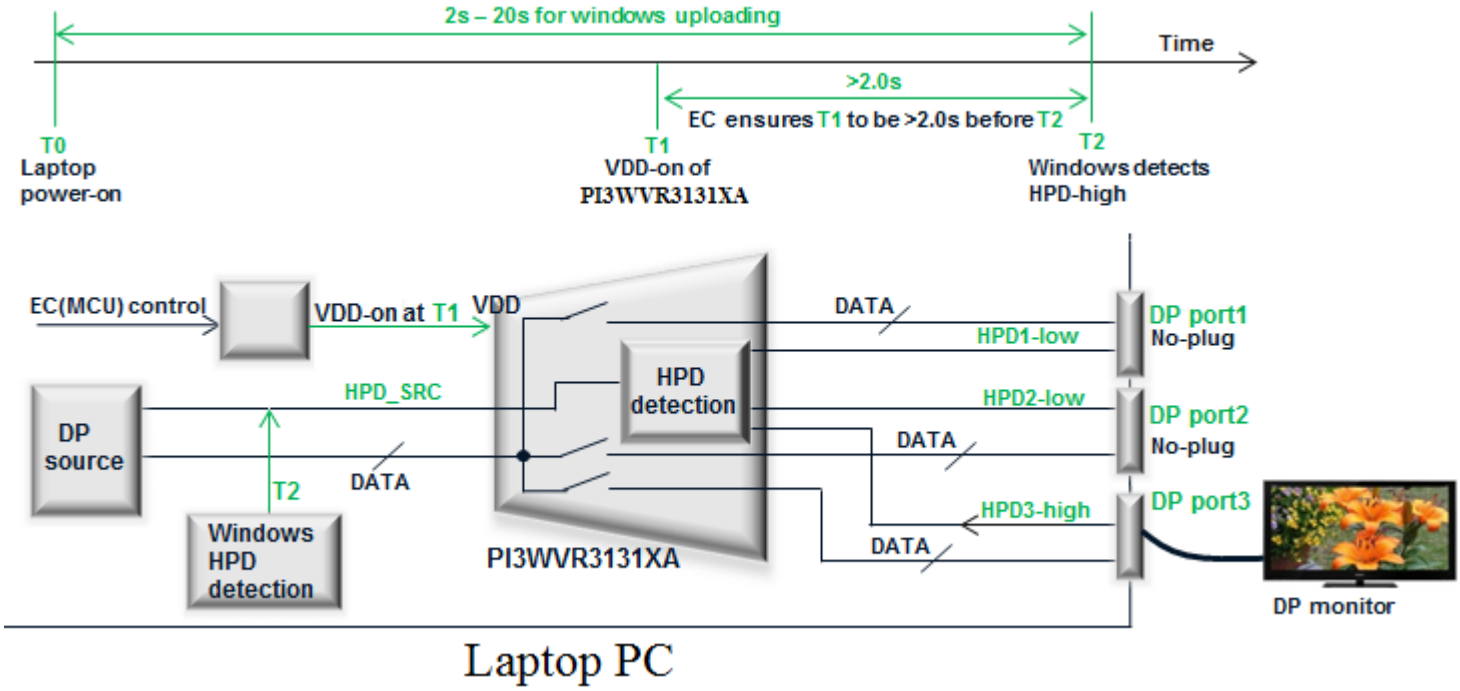


Figure 14, the recommended system timing for PI3WVR313XA

9.0 Power and power de-coupling

Use 0.1uf in size of 0402 for all the Vdd (any power pins) pins of the IC device, as close to the Vdd pins as possible, within 2-3mm if feasible.
Use dedicated Vdd and GND planes for to minimize the jitters coupled between channel trough power sources.

10 Layout guideline

10.1 Recommend 90 ohm differential impedance trace for differential DP and USB 3.0 signals

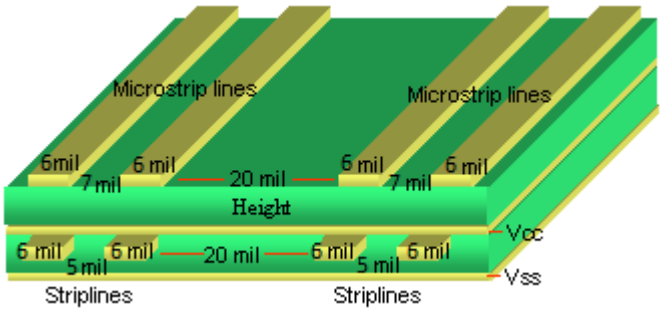


Figure 15, the trace width and clearance

- Use 6-7-6 mils for trace-space-trace for the micro-strip lines (the traces on top and bottom layers) for 90 ohm differential impedance.
- Use 6-5-6 mils for trace-space-trace for the strip-lines (the traces inside layers) for 90 ohm differential impedance.
- Use FR4.
- Using standard 4 to 8 layers stack-up with 0.062 inch thick PCB.
- For micro-strip lines, using ½ OZ Cu plated is ok.
- For strip-lines in 6 plus players, using 1 OZ Cu is better.
- The trace length miss-matching shall be less than 5 mils for the "+" and "–" traces in the same pairs
- More pair-to-pair spacing for minimal crosstalk
- Target differential Zo of 90 ohm ±15%

10.2 The PCB Layers Stackup

- No new PCB technology required. Use FR4 is fine.
- Using standard 4 to 8 layers stack-up with 0.062 inch thick PCB.
- For micro strip lines, using ½ OZ Cu plated is ok.
- For strip line in 6 plus players, using 1 OZ Cu is better.

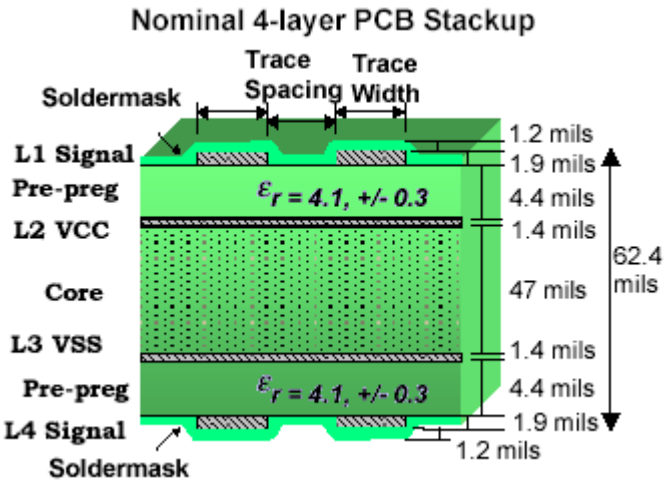


Figure 16, the stackup

Stack-up

Plane	Material	Thickness (mil)
Solder mask	Mask paint	1.2
Signal	Copper	1.9
Prepreg	2116	4.4
Vcc	Copper	1.4
Core		47
Vss	Copper	1.4
Prepreg	2116	4.4
Signal	Copper	1.9
Solder mask	Mask paint	1.2
Total		62.4

10.3 The Layout Guidance for the Trace Routings

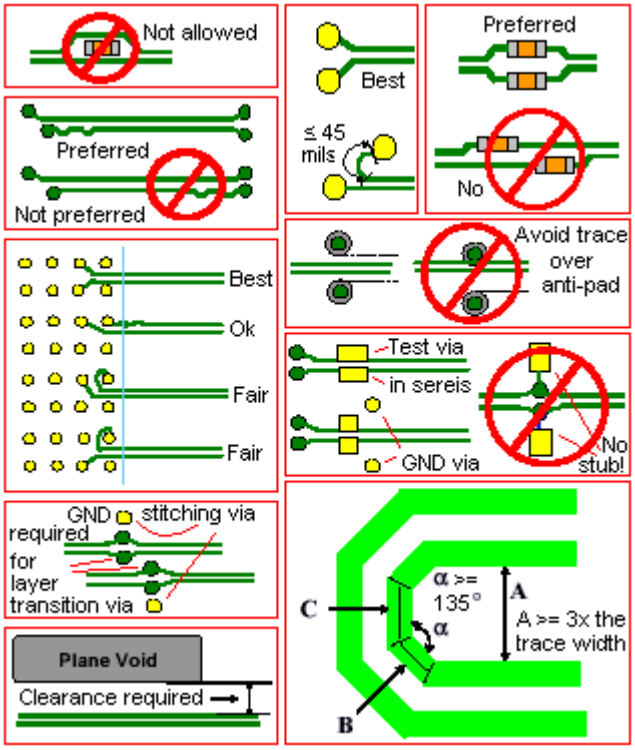
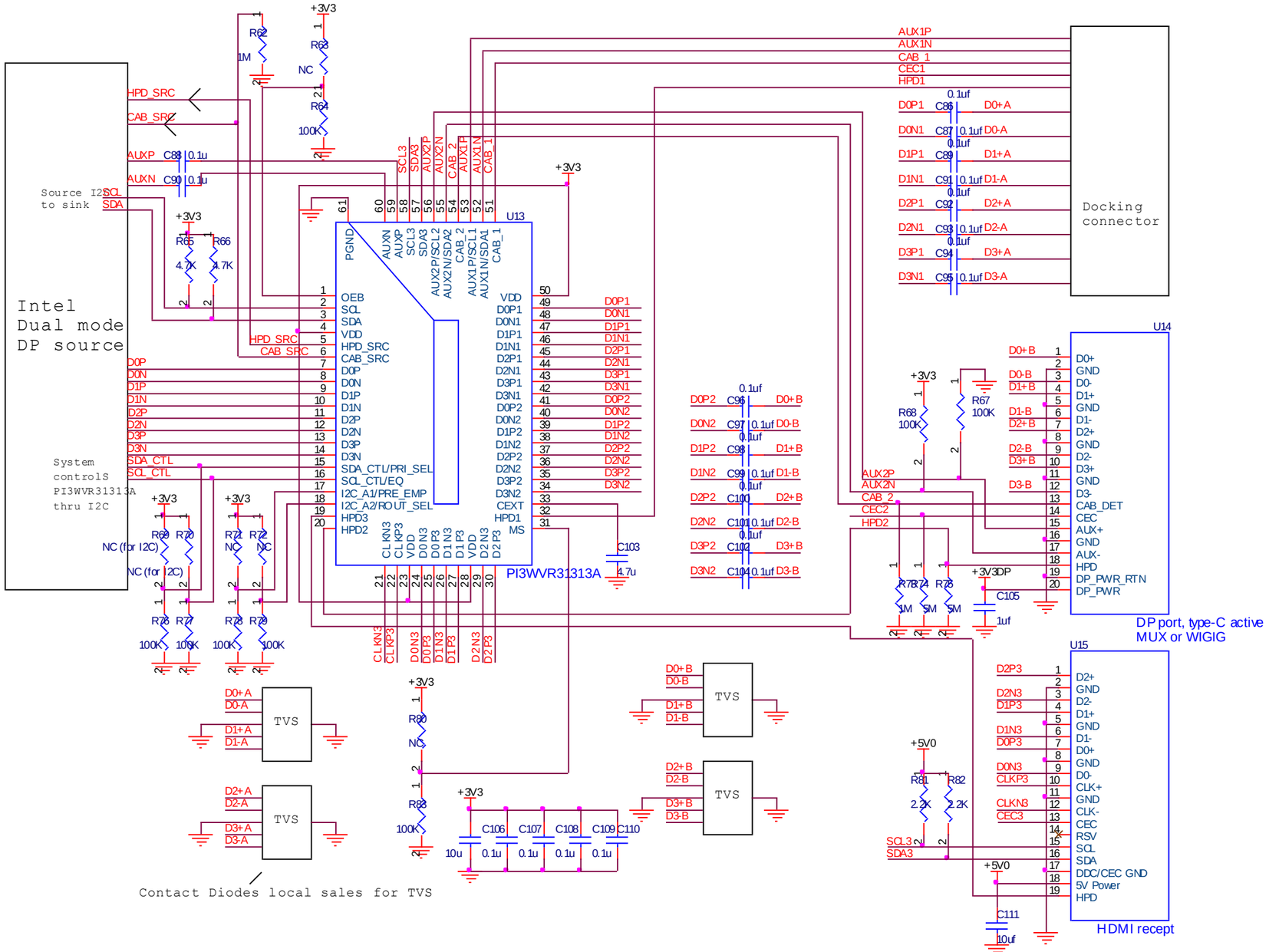


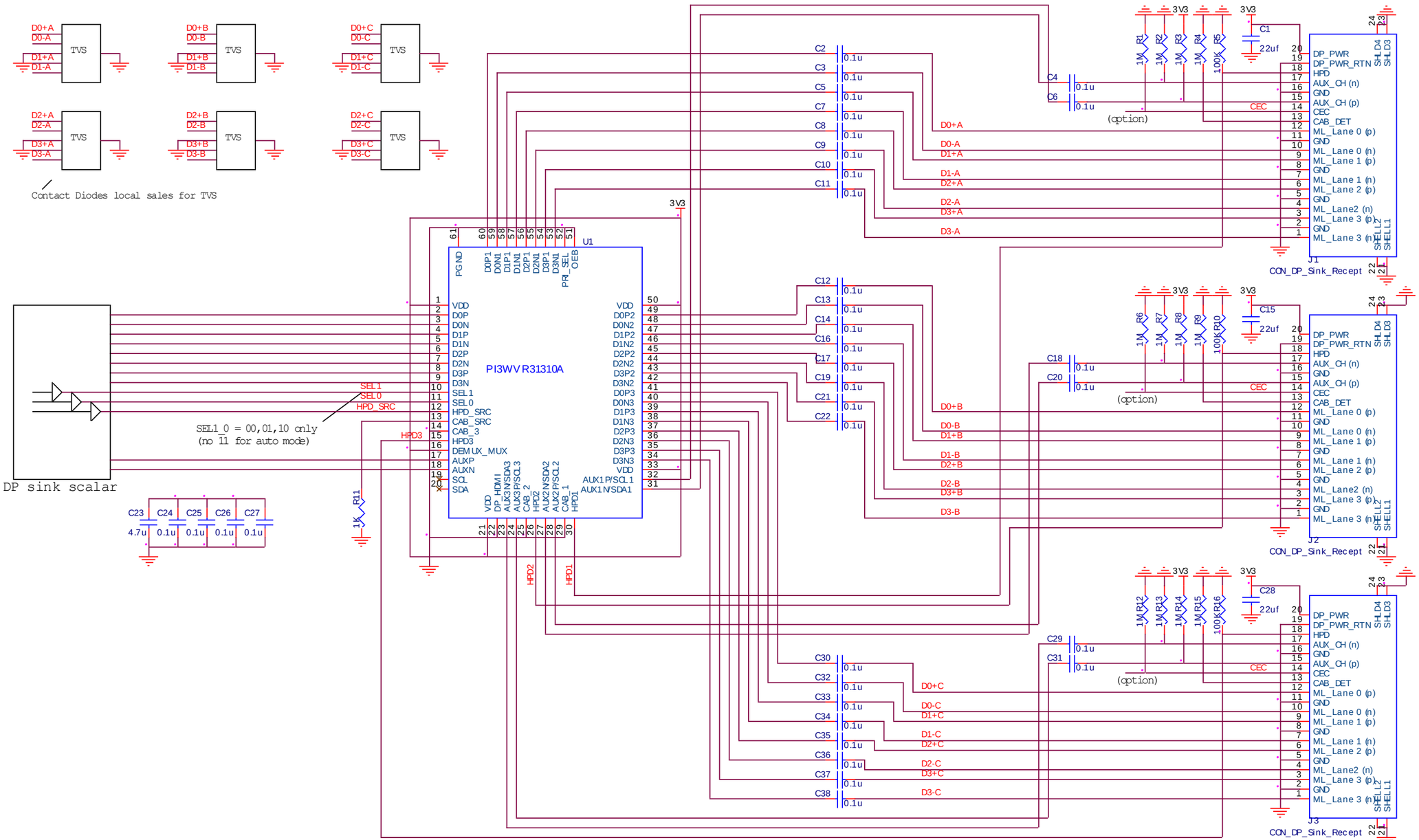
Figure 17, The layout guidance for the trace routings

- Don't use EMI chokes for passive switch channels, which do have have EMI issues.
- The differential traces shall be away from the strong EMI source and devices, such as TTL, switching-power traces and devices, with at least 30mil to 50mil space.
- No other components shall piggy ride on the differential traces.

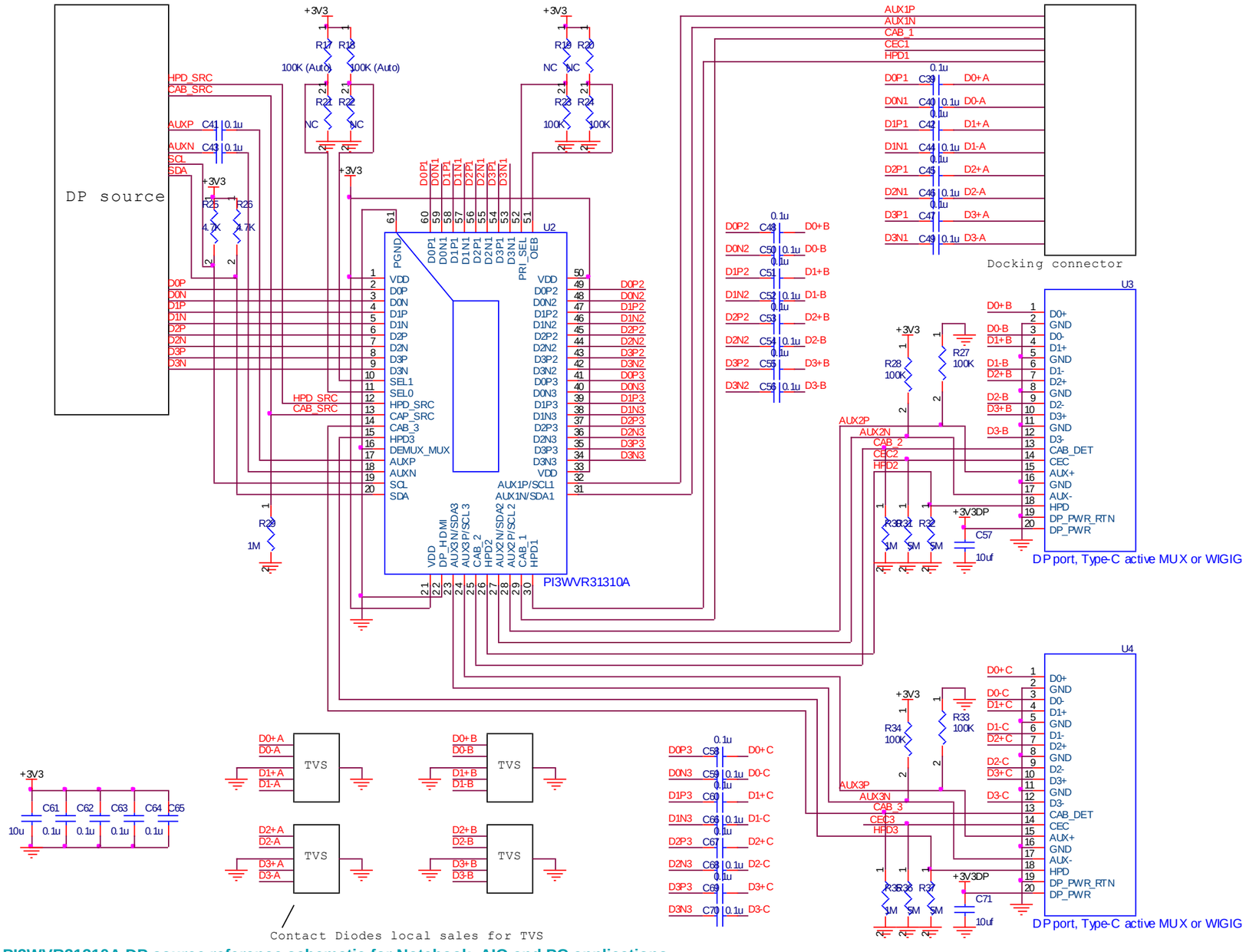
11 Appendix: application Reference Schematics



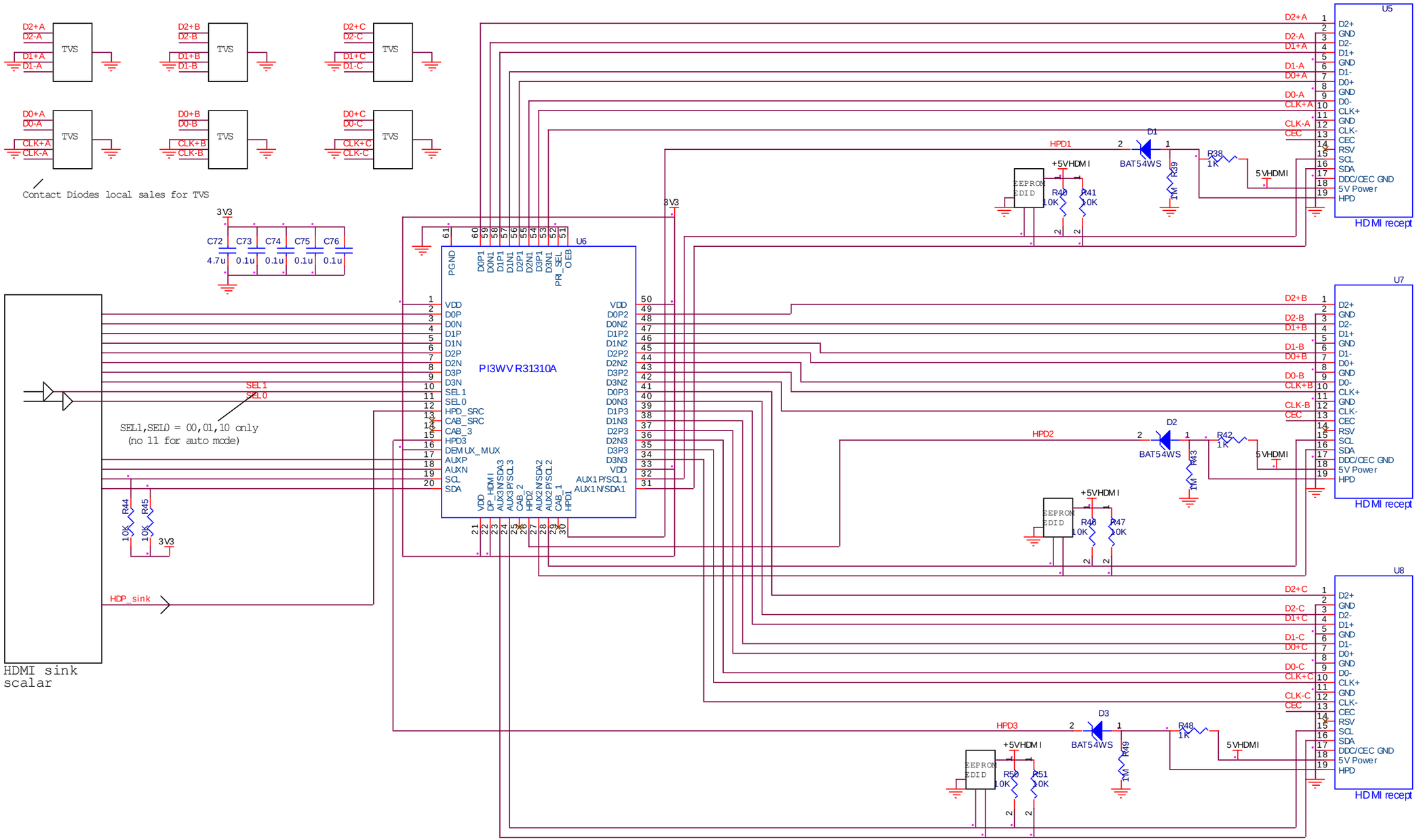
PI3WVR31313A DP++ source reference schematic for Notebook, AIO and PC applications



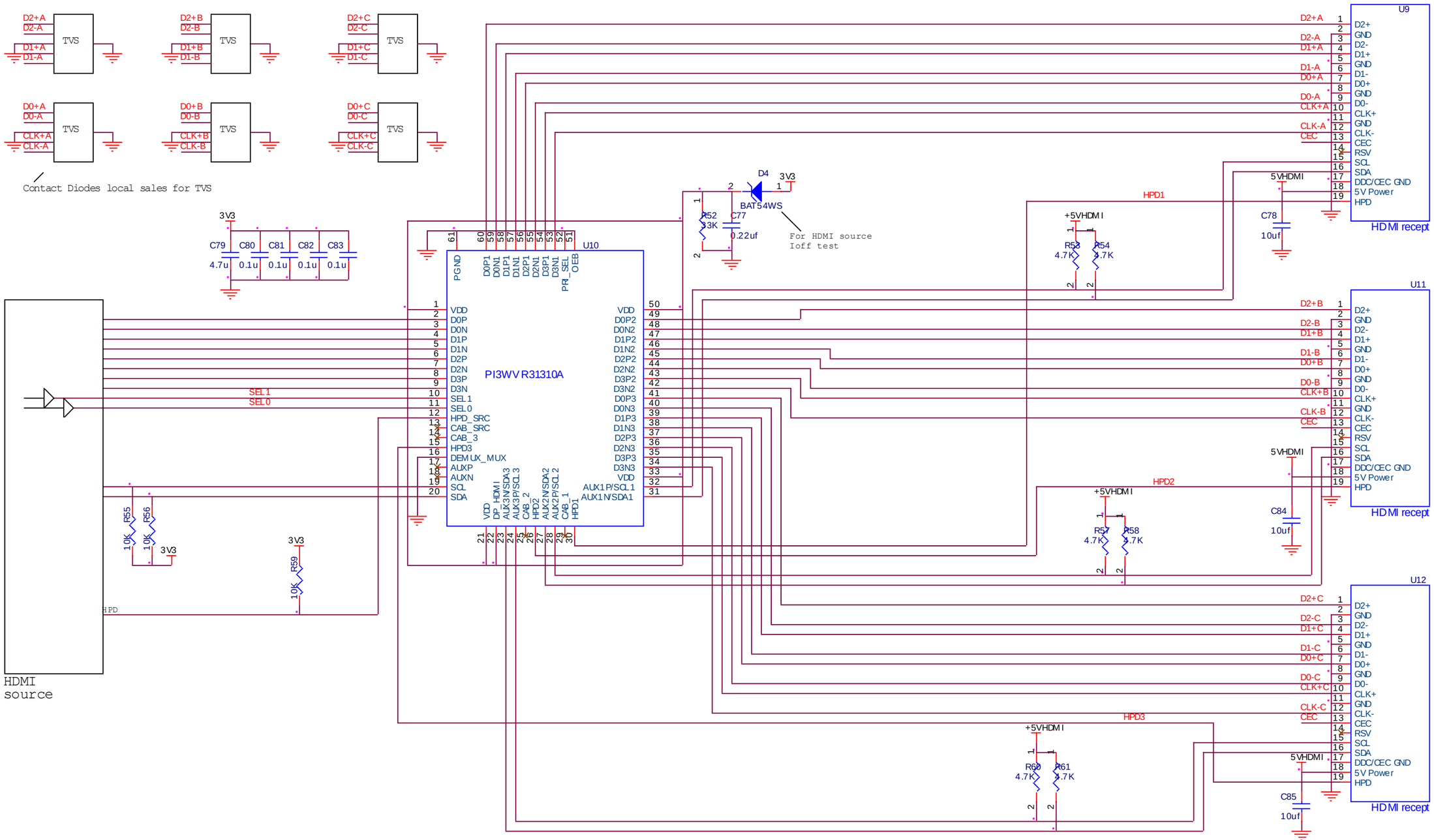
PI3WVR31310A DP sink reference schematic for DP monitor applications



PI3WVR31310A DP source reference schematic for Notebook, AIO and PC applications



PI3WVR31310A HDMI sink reference schematic for HDMI monitor and HDTV applications



PI3WVR31310A HDMI source reference schematic