

Design Guidance for AP3106

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1. Introduction

The AP3106 is a high voltage start-up, current mode PWM controller with green-mode power-saving operation.

The PWM switching frequency at normal operation is externally programmable and trimmed to a narrow range. The AP3106 integrates a proprietary internal frequency dithering function that helps to reduce EMI emission of a power supply with minimum line filters used.

To minimize the standby power consumption, a proprietary adaptive green-mode function is available to implement frequency modulation under light-load conditions. To avoid acoustic noise problems, the

minimum PWM frequency is set at about 26kHz.

The AP3106 integrates a lot of functions such as the Lead Edge Blanking (LEB) of the current sensing, internal slope compensation, line compensation, and several protection features that include cycle-by-cycle current limit, OVP, OTP, OLP and brownout protection.

The AP3106 is available in SOIC-7 package to realize a compact size.

2. Function Block Description

The detailed information of the function block is shown in Figure 2.

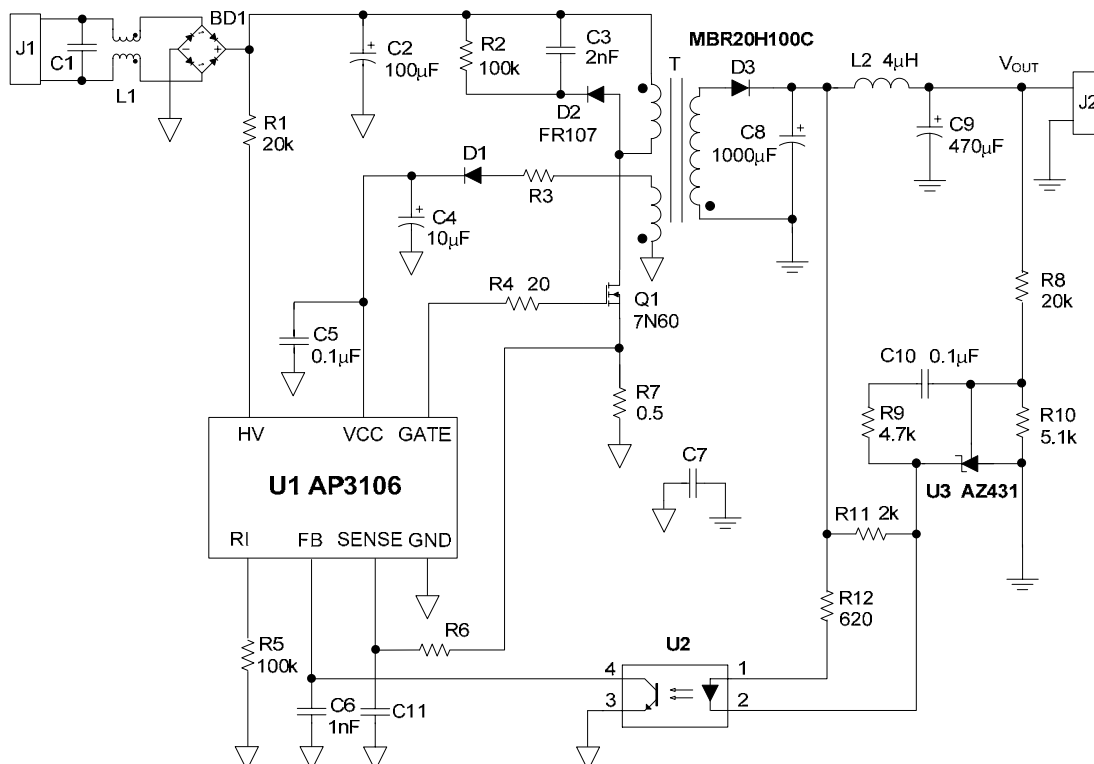


Figure 1. System Schematic Circuit with AP3106

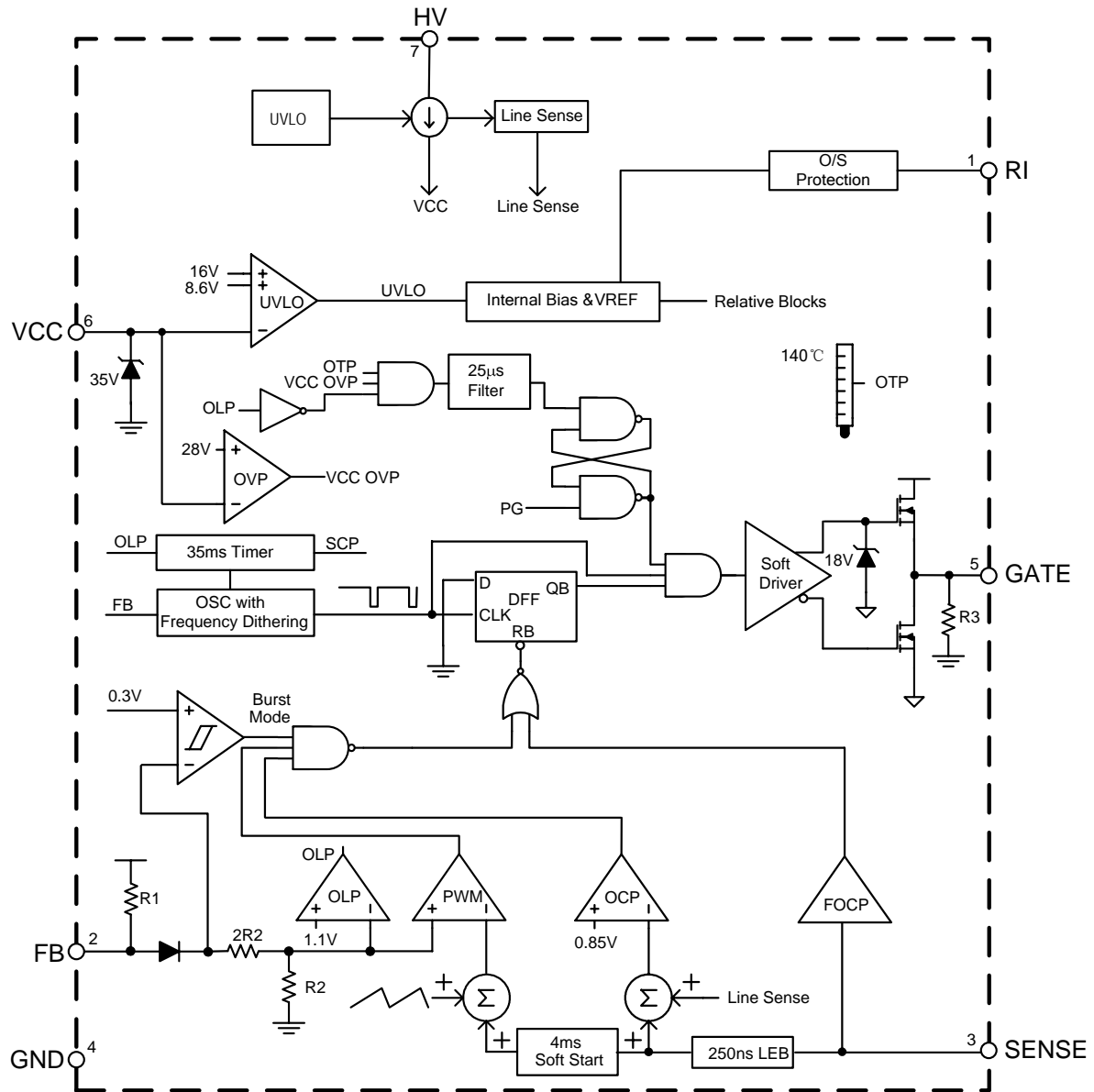


Figure 2. Functional Block Diagram of AP3106

3. Operation Information

3.1 Start-up Circuit and UVLO

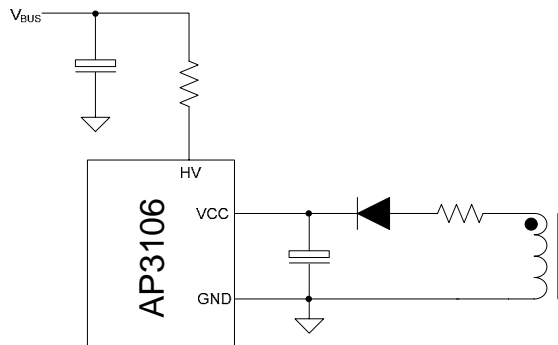


Figure 3. Start-up Circuit for Converter

To get low standby power consumption and achieve quick start-up performance, the AP3106 is designed to incorporate a high-voltage start-up circuit. During start-up, an internal 1.3mA current source is drawn from bus capacitor to charge the VCC holdup capacitor via a start-up resistor. As the VCC reaches the UVLO (on), the IC is activated and the high voltage start-up circuit is turned off. Then the IC is supplied from the auxiliary winding of the transformer.

The AP3106 incorporates an UVLO comparator to detect the VCC. It ensures VCC holdup capacitor enough energy to supply AP3106 when powering on. The turn-on threshold is 16V while the turn-off threshold is 8.6V.

3.2 Oscillator and Frequency Dithering

The oscillation frequency can be set by the resistor on RI pin. The resistor will produce a constant current source to determine the oscillation frequency by charging and discharging an internal capacitor. Normally, the resistor should be placed as close to the IC as possible to avoid noise disturbance that may cause abnormality to the IC.

The oscillation frequency can be expressed as:

$$f = \frac{6500}{R_{RI} \text{ (k}\Omega\text{)}} \text{ (kHz)}$$

The oscillation frequency is recommended to be from 50 to 100kHz with the consideration of EMI.

The AP3106 features a frequency dithering function to provide designers an optimized EMI performance with just a few EMI components at the lowest cost.

3.3 FB Input

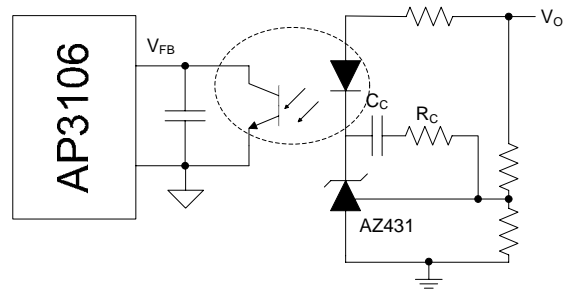


Figure 4. FB Pin Connection for Closed Loop Control

The FB pin is used for closed-loop control of the whole system. The typical feedback circuit consists mainly of a shunt regulator and an opto-coupler. RC and CC are used for control loop compensation. One capacitor should be always placed on the FB pin to achieve better stability. Under current mode control, the VFB controls the peak inductor current to meet the output power:

$$I_{PEAK} = \frac{V_{FB} - 0.9}{3 \times R_S}$$

Where IPEAK is the peak inductor current, VFB is the voltage on the FB pin, RS is the current sense resistor and the internal divider ratio is 3.

When VFB is larger than 4.2V and lasts for about 35ms, the IC will enter the protection mode. If the VFB is less than 0.9V, the driving pulse will be also terminated immediately, which can be applied for other protection.

3.4 Current Sense Comparator and LEB

The AP3106 is a current mode controller. Its output driving signal is initiated by every oscillating cycle and is terminated when the IPEAK reaches the threshold level determined by the FB pin.

A narrow spike on the leading edge of the current waveform can be usually observed when the power MOSFET is turned on. The spike is mainly caused by the secondary schottky reverse recovery as well as the discharging of the parasitic capacitor of MOSFET and the transformer. So a 250ns leading edge blank has been built-in to prevent the false triggering caused by the turn-on spike. During the LEB, the current limit comparator is disabled and the gate

driver can not be turned off. A small RC filter is recommended to be connected to the CS pin to avoid the damage to this pin by the negative turn-on spike.

3.5 Built-in Slope Compensation

It is well known that SMPS may become unstable when the duty cycle exceeds 50% in Continuous Current Mode (CCM). The built-in slope compensation can reduce the current loop gain to stabilize the system in CCM without extra external components. A synchronized compensation ramp is added onto the current sense signal compared with feedback to get the output pulses.

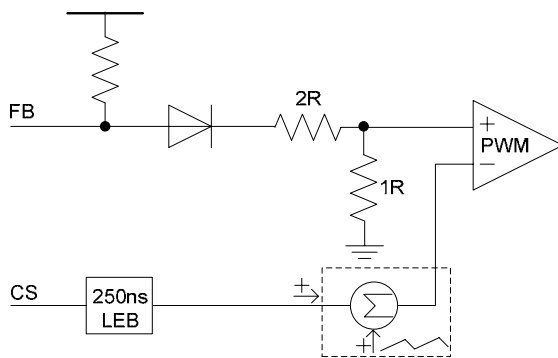


Figure 5. Slope Compensation Circuit

3.6 Frequency Fold-back

As we know, the switching loss is significant at light load, and is proportional to the switching frequency. The AP3106 features frequency fold-back to reduce the switching frequency to improve the efficiency at light load, and this is also helpful to improve the average efficiency. The minimum frequency should be more than 20kHz to avoid the interference from audio frequency.

3.7 Line Compensation

As the load increases, the peak inductor current increases accordingly. When the peak inductor current reaches the threshold, the OCP is triggered and the system is protected cycle-by-cycle. Once the OCP occurs, the output pulses are terminated after a small propagation delay, which results in different power limit under universal AC input. The AP3106 has built-in line compensation to ensure a constant power limit. As shown in Figure 6, the current limit signal, which is changing in accordance with the line voltage, is added onto the inverting input of the OCP

comparator. So the current limit of low input voltage is higher than the high input voltage. With the same propagation delay, the actual current limit is the same under universal AC input.

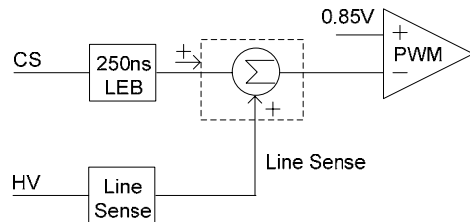


Figure 6. Line Compensation Circuit

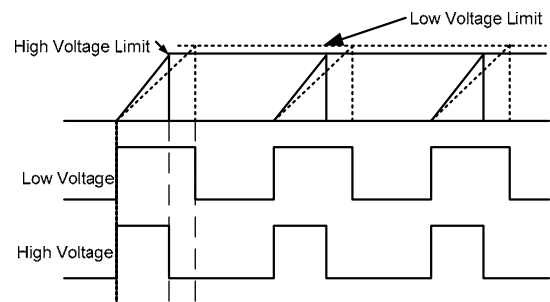


Figure 7. Constant Output Power Limit

3.8 Built-in Brownout Protection

The AP3106 has a built-in comparator for brownout detection as shown in Figure 8. Once abnormal line voltage is detected, the controller is shut down to prevent the damage. As shown in Figure 9, when the line sense signal is below 1.1V, the driving signal is terminated. The brownout protection is released till the line sense signal exceeds 1.15V. Then the system returns into normal operation.

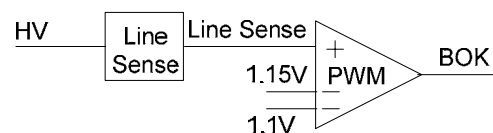


Figure 8. Brownout Protection

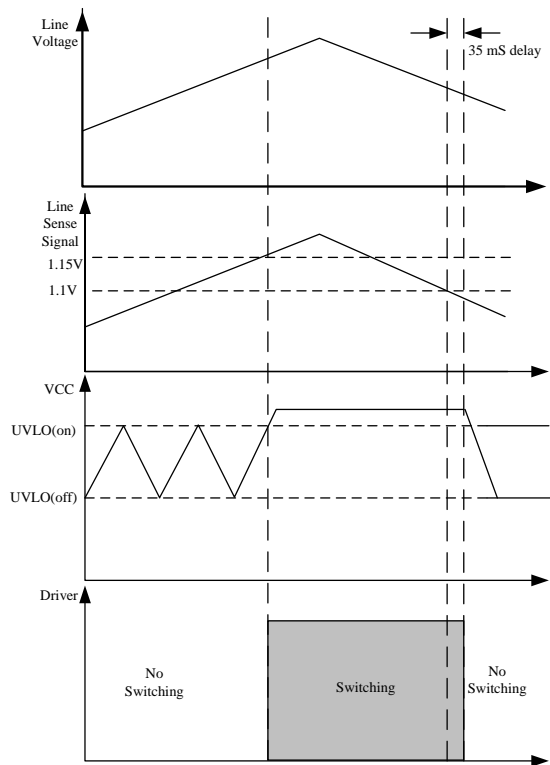


Figure 9. Waveforms during Brownout Protection

3.9 Over Load Protection (OLP)

The AP3106 features OLP function to protect the system being damaged under over-load or short-circuit condition. If the output reaches the maximum output current, the output voltage drops and the feedback error amplifier is saturated with V_{FB} going up to a high level. Once the voltage exceeds the threshold and lasts for more than 35ms, the OLP is activated to terminate the switching pulses.

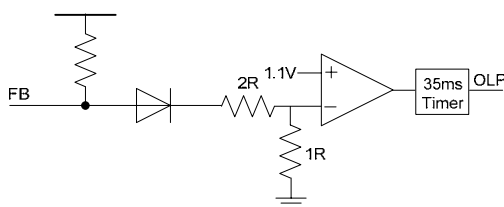


Figure 10. OLP Circuit

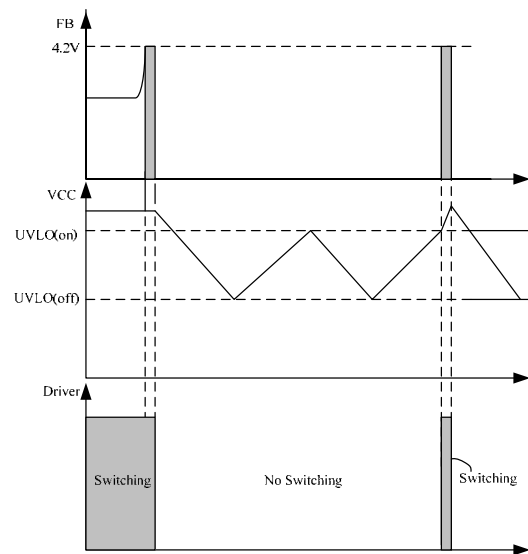


Figure 11. Waveforms during OLP Protection

As shown in Figure 11, once V_{FB} reaches 4.2V and lasts for more than 35ms, UVLO is triggered for 2 times to protect the whole system, which can be used to reduce the input average power under OLP or short-circuit condition. So the component temperature and voltage stress fall into a safe and controllable range.

3.10 VCC Over Voltage Protection (VOVP)

The VOVP is an auto-recovery protection. As shown in Figure 12, as long as the VCC voltage is higher than OVP threshold, the driving signal is terminated and the whole system is shut down. The system will restart until next UVLO (on). Once VCC voltage is lower than OVP threshold, the VOVP status will be released with the system returning into normal operation. The VOVP is usually caused by the open feedback loop.

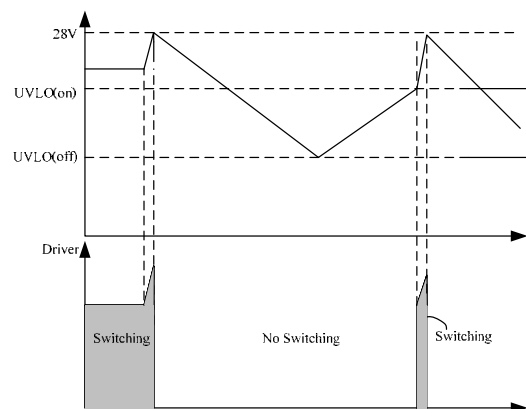


Figure 12. VOVP Protection

3.11 Fast OCP for Secondary Short-circuit Protection

When the load is short-circuit, the power converter can be protected by OLP. But if the output filter inductor or the secondary schottky is short-circuited, the transformer will be immediately saturated resulting in the breakdown to the MOSFET due to high voltage stress.

The AP3106 has built-in fast OCP function to alleviate the saturation of transformer and reduce the voltage stress of MOSFET. As showed in Figure 13, with fast OCP, the power converter can operate normally even the secondary schottky and the output filter inductor is short-circuited.

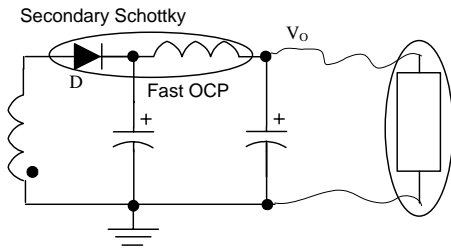


Figure 13. Fast OCP Protection

3.12 Audible Noise Consideration

Audible noise, which mainly comes from the transformer and snubber capacitor, is usually a common issue in SMPS applications.

For the noise caused by transformer, it is mainly due to unstable loop and burst-mode frequency as shown in Figure 14. There must be audible noise frequency (normally from 2kHz to 20kHz) in the unstable loop. The noise from unstable loop can be eliminated by adjusting the loop compensation. For burst-mode frequency, which is unavoidable, one way is to use good adhesive to fix each part of the transformer, another way is to minimize the flux density variety that could be done by reducing the maximum primary current under burst mode or minimizing the primary inductance properly.

The audible noise caused by snubber capacitor is due to the electrostrictive and piezoelectric effect in some ceramic capacitor under alternative electric field intensity. And the solution is to use film or other polypropylene capacitor.

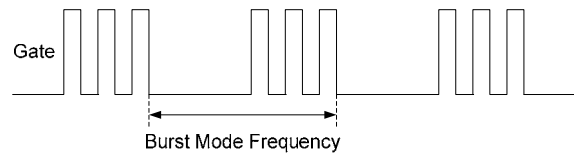


Figure 14. Burst Mode