AN53
DC-DC PoL conversion using Zetex' ZXMN2F34MA MOSFET

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Introduction

The functionality of telecom, industrial and other general purpose systems that use a microprocessor or ASIC have become increasingly sophisticated, placing ever more stringent demands on power density and dissipation of the Point of Load ('PoL') power supply within them. This application note describes the use of the ZXMN2F34MA in a synchronous buck converter as shown in Figure 1, which is suitable to be used as a PoL power supply. Housed in the leadless DFN322, the ZXMN2F34MA offers superior thermal performance, improved silicon to footprint ratio and a lower profile than its leaded surface mount predecessors. The ZXMN2F34MA measures 2mm by 2mm, 0.85mm height and has a PCB footprint of only 4mm^2-half that of the industry standard SOT23 package. Furthermore, it has a thermal resistance that is 40% lower than that of a comparable SOT23 device, enabling the MOSFET to deliver a superior thermal performance from a footprint that is half the size of the SOT23.

Package information

The thermally optimized DFN322 package as shown in Figure 2, is made using a highly conductive copper alloy metal pad as the 'die attach pad' which is exposed and soldered directly to the outside of the package. This enables an excellent thermal path for heat to be removed from the die (junction) to the board and is consequently characterized by very low thermal impedances R_{thjc} and R_{thja}, resulting in excellent thermal/ electrical grounding to the printed circuit board.

The interconnection between die and drain pad is performed by a high conductivity adhesive which ensures a reliable die contact. The interconnections from source and gate die pad to the wire bond pads (leads) is optimally fabricated using gold wires.

The majority of the heat flow will travel from the exposed drain pad via the printed circuit board. An effective way to increase the power capability of the device in this instance is to increase the landing pattern on the PCB, add vias and increase the weight of copper. When housed in such a package, a power MOSFET can either have higher current handling capability or operate with a lower junction temperature. The benefits of cooler operation are higher efficiency due to the MOSFET having a lower $R_{DS(on)}$, which in turn means a reduced conduction loss. A further benefit of cooler operation is that a reduced junction temperature of just 10°C could, in fact, double the lifetime reliability.

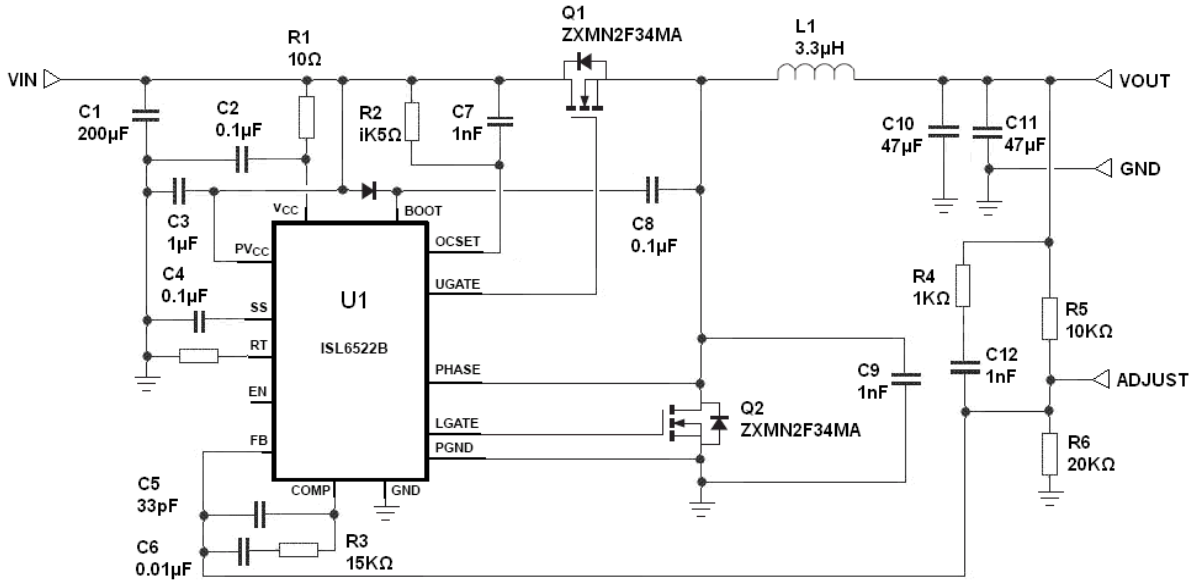

Figure 1 Synchronous buck PoL converter using ZXMN2F34MA

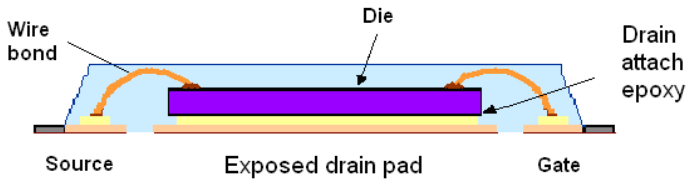

Figure 2 Cross-section of the DFN322 package

In addition to the package resistance, the die-free package inductance, especially the drain inductance, is reduced when compared to standard SOT23 or SO8, a consequence of the short bond wire and external lead length. The lower package inductance provides benefits in term of faster switching speed, reduced peak drain-source voltage ringing at high frequency and lower EMI emission. These features make the ZXMN2F34MA suitable for use in high switching frequency PoL conversion, where PCB footprint, thermal performance and high efficiency are of prime importance.

Low voltage MOSFET: Considerations for synchronous buck converter

Synchronous buck converter is generally the topology of choice for a non-isolated point of load converter, to convert a high input voltage into a lower output voltage. In the synchronous buck converter, the forward voltage drop of a Schottky diode in a normal buck converter is replaced by the MOSFET low $R_{DS(on)}$ loss to improve efficiency.

For the following discussion, the ZXMA2F34MA is considered for a nominal 12V input 1.2V output PoL converter, capable of delivering up to 3A load current. This kind of converter is commonly used in power management applications that require high efficiency, tight regulation, and high reliability in elevated temperature environments with low airflow.

As shown in Figure 1, the converter comprises the control FET (Q1), synchronous FET (Q2), PWM controller (U1) and output inductor (L1). U1 is selected based on its ability to supply sufficient current to drive the two N-channel MOSFETs at high frequency and, the controller needs to provide simple, single feedback loop, voltage mode control with fast transient response. L1 inductance needs to satisfy both the output voltage ripple and load transient response time requirements. Increasing the value of L1 will reduce the ripple current and ripple voltage across the load, at the expense of increasing the converter's response time to transient load change.

The majority of the power lost in synchronous buck power conversion is due to the MOSFET, and is generally noticeable as:

- MOSFET conduction losses
- Switching losses of MOSFET
- Source-drain diode conduction and reverse-recovery losses

In order to maximize the performance of this power supply, it is necessary to minimize these loss components. The low output voltage buck converter has low duty cycle, concentrating the majority of the conduction loss on the synchronous FET (Q2). In fact, the conduction duty cycle of Q2 could be as high as 90% for a 1.2V output, so the primary selection criteria for this MOSFET should be low $R_{DS(on)}$. The switching loss in Q2 is negligible since the transistor turns on and off with only a diode voltage drop across it.

In contrast, the control FET Q1 has a much shorter duty cycle and its conduction loss has less of an impact on overall efficiency. Since Q1 is operated at a switching frequency above 300kHz and approaching 1MHz, capacitive and switching loss surpass conduction loss, a low gate charge MOSFET needs to be used for Q1.

By optimizing the cell density for the given breakdown voltage, ZXMN2F34MA has a $R_{DS(on)}$ value of only 60mΩ at 2.5A drain current, whilst its low gate charge Q_g = 2.8nC is achieved through an increase in the gate oxide thickness and optimization of the gate overlap area to reduce the input capacitance. The modulation of these parameters facilitates optimization of the ZXMN2F34MA performance, making it imminently suitable to be used as both control and synchronous FETs in the buck converter.

A synchronous buck driver generally inserts a finite dead time of 20 to 80ns which precedes the turn on and follows the turn off of Q2 to prevent shoot through, especially on the low to high transition. During this time, the load current is forced into the source-drain diode. The source-drain diode subsequently has to recover its own stored charge at the turn on transition of Q1, which will contribute to the MOSFET losses.

Q_{rr} and t_{rr} are important parameters and can contribute significantly to the high side FET efficiency and current stress. A high Q_{rr} will necessitate Q1 to be de-rated to handle the extra current during recovery. In order to address these issues, the drain-source diode's carrier lifetime in the ZXMN2F34MA has been optimized to achieve low Q_{rr} to ensure low MOSFET's temperature rise and to circumvent the need for a bypass Schottky diode in parallel with Q2. Furthermore, if an external Schottky diode is used, its capacitance needs to be charged during the turn on switching of Q1 which adds to the total converter losses. Table 1 details the electrical characteristic of the source drain diode within the ZXMN2F34MA.

Table 1 Source drain diode characteristics

Parameter	Symbol	Typ.	Unit	Conditions
Reverse Recovery Time	t_{rr}	6.5	ns	I_s = 1.65A; T_j = 25°C; di/dt = 100A/µs
Reverse Recovery Charge	Q_{rr}	1.4	nC	
Diode Forward Voltage Drop	V_{SD}	0.73	V	I_s=1.25A; V_{GS}=0V

More details on MOSFET power losses consideration can be found in the Appendix.

Figure 3 shows measured efficiency data for 12V input 1.2V output converter with the ZXMN2F34MA to demonstrate the implementation of a non isolated PoL converter operating at 330kHz switching frequency, as discussed in the previous section.

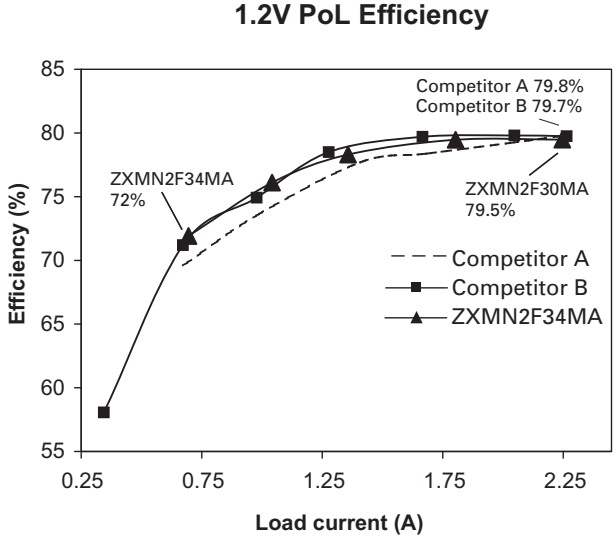

Figure 3 12V input, 1.2V output PoL converter efficiency

The performance of the ZXMN2F34MA in the PoL converter is compared with that of the competitor A, a 4.7A, 30V trench MOSFET in the industry standard SOT23 package and, the competitor B, which is a 5.6A, 30V MOSFET in the SC70-6 package. The efficiency of the resulting converters approaches 80% at high load current. Under light load condition, the efficiency drops to around 70% as the circuit loss is dominated by losses due to capacitive switching which is not a function of the load current. From Figure 3, it is observed that the performance difference between the ZXMN2F34MA and the competitors' parts is less than 0.4% efficiency. It must be noted that the ZXMN2F34MA, whilst housed in such a small package, has managed to achieve comparable efficiency to competitor MOSFETs which are housed in much bigger packages.

Conclusion

For low current and high density application, the MOSFET package selection and power dissipation are the dominant design criteria for a PoL DC-DC converter. The DFN322 package combines high performance silicon with space savings, enabling a designer to increase the power density without compromising performance, incurring higher BOM cost or adding complexity to the manufacturing process. These features make the ZXMN2F34MA suitable for use both as high and low side switches in high switching frequency PoL converters, where PCB footprint, thermal performance and low threshold voltage are of prime importance.

Appendix

This section provides more detail on the MOSFET loss estimation in synchronous buck converter. Control (Q1) conduction loss:

$$P_{ON(Q1)} = I_{OUT}^2 * R_{DS(on)} * D$$

where $R_{DS(on)}$ is at the operating junction temperature T_J and $D = V_{OUT} / V_{IN}$, is the duty cycle of the buck converter. The $R_{DS(on)}$ value is influenced by the gate-source voltage value as well as the junction temperature, where the resistance typically has a positive temperature coefficient of around 0.4%/°C.

The switching loss in Q1 inclusive of both rising and falling edges:

$$P_{SW} = (V_{DS} * I_{D(Pk)} * f * (t_{ON} + t_{OFF})) \div 2$$

Most of the time during the switching interval of Q1 is spent charging/discharging the MOSFET Miller capacitance. The switching time can be calculated from the gate charge Q_g and the PWM controller's source and sink current:

$$t_{ON} = Q_g \div I_{SOURCE}$$

$$t_{OFF} = Q_g \div I_{SINK}$$

The power to charge/discharge Q1's C_{OSS} output capacitance during switching transition:

$$P_{COSS} = C_{OSS} * V_{IN}^2 * f \div 2$$

Ignoring the effect of the gate charge Q_{TH} required to reach the MOSFET threshold voltage, Q_g equals to the summation of and the charge supplied to the gate-source Q_{gs} and Q_{gd}. The power loss required to charge/discharge the gate is distributed between the driver internal pull up resistor, gate damping resistor and MOSFET internal gate resistor:

$$P_G = Q_g * V_{GS} * f$$

A high gate source voltage V_{GS} should be used to reduce $R_{DS(on)}$, this , however, is done at the expense of incurring a greater gate charge, thereby there is a trade-off between conduction and capacitive losses in the power switching circuit. However, the gate charge loss is mainly dissipated in the controller and will not heat up the MOSFET.

The body of synchronous MOSFET (Q2) turns on and off with its drain source diode conducting, therefore $V_{DS} \approx 0.7V$. Q2 is primarily selected based on conduction loss given by,

$$P_{ON(Q2)} = I_{OUT}^2 * R_{DS(on)} * (1 - D)$$

Loss in source drain diode due to reverse recovery loss can be estimated by,

$$P_{Qrr} = V_{IN} * Q_{rr} * f$$

The magnitude of the reverse recovery loss can be reduced by slowing down Q1's turn on speed to reduce the di/dt slope, or by selecting a controller which has the minimum dead-time. A controller that truncates the dead-time will reduce reverse recovery effect by limiting energy stored in the diode. The source-drain diode forward conduction loss is a function of the dead time:

$$P_D = V_F * (I_{out} - (\Delta i_L \div 2)) * t_{dead} * f$$

Unless the switching frequency is very high, the loss contribution due to the dead-time diode conduction is minimal.

To ensure that both MOSFETs are within their maximum junction temperature at elevated ambient temperature, calculate the temperature rise according to the above power loss equations and the ZXMN2F34MA package thermal resistance specifications.

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