DN1156

Gate Drivers in BLDC Motors

Three-phase Half-bridge Driving Brushless DC (BLDC) Motor

The Brushless DC (BLDC) motor market is expected to grow over the next few years for a few reasons. First the growth of new industries like drones (UAVs), E-bikes, and RC vehicles has highlighted the versatility and increased efficiency of BLDC motors. The increasing performance of batteries and BLDC motors is well suited for the hand held power tools market. Also in consumer applications, government standards are requiring better efficiency appliances. This is making appliance manufacturers to use BLDC motors for the compressors, fans etc. Also consumers and companies are demanding better efficiency for lower long term cost. Hence for many applications (white good appliances, air conditioners, industrial automation) older lower efficiency AC motors are being replaced by higher efficiency BLDC motors. All BLDC motors require electronic control to provide the appropriate switching voltage and currents to drive the motor. Since the switching element is typically a MOSFET or IGBT, the Diode's gate drivers are a perfect choice for BLDC motor driver applications.

Three-phase motor configurations are becoming the most common motor configuration. Figure 1 is a 3-phase half-bridge configuration using MOSFETs to drive voltage and current lines to a 24V BLDC motor. The MCU provides three logic level PWM signals to the inputs of three DGD2104, Half-Bridge Drivers. The DGD2104 translates this logic level to a low-side MOSFET gate drive and a floating high-side MOSFET gate drive. The DGD2104 inserts an internal dead time of 520ns to protect the MOSFETs from shoot-through: a situation in which both MOSFETs are on at the same time causing the power bus rail to be shorted to GND that wastes power and could damage the MOSFET. BLDC motors commonly work with 12V, 24V, 36V, or 48V line voltages. This enables the designer to use more inexpensive MOSFETs that also may have lower R_{DS}(on). For an offline power source a power supply is required to produce the stable 24V supply, but the lower DC voltage required to drive these motors, are perfectly suited for battery driven applications like UAVs and power tools.

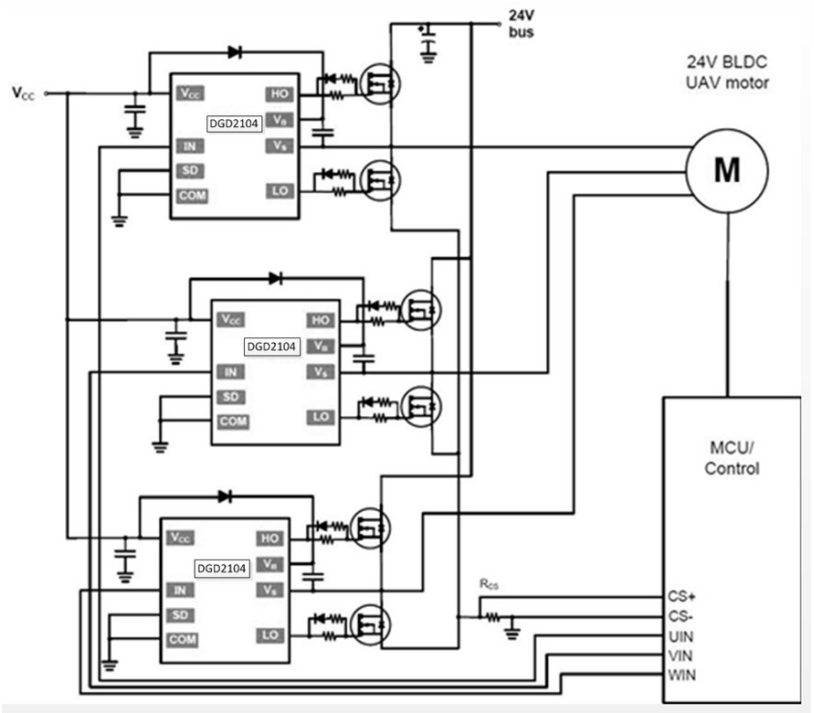

Figure 1: General Schematic of Three-Phase Inverter BLDC Motor Driver

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Half-bridge Circuit Design for Motor Driver

Figure 2 shows an example circuit design for a single-phase half-bridge that may be used in the BLDC motor drive of Figure 1. The gate resistors (the 50Ω source drive and the 10Ω sink drive) are chosen to slightly decrease the rise time to minimize noise in the highly noisy environment of motors. Also the larger decoupling cap and bootstrap capacitor (2.2µF) are chosen to maintain a steady supply during high dI/dt switching times.

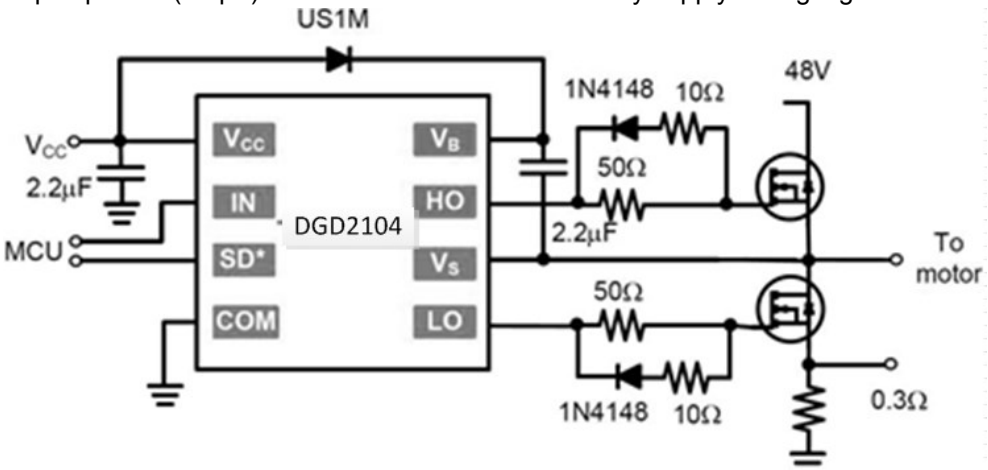

Figure 2: Example Circuit Design for the Half-Bridge Driver for BLDC Motor Applications

Gate Driver Design Note

The aim of this Design Note is to provide more detailed data for the designer of a motor drive board using Diode's gate drivers. First an example design is given for a half-bridge to use in a 3-phase BLDC motor drive circuit. For the remainder of the Design Note, the important parameters to consider (gate resistor selection, bootstrap capacitor selection, layout considerations etc.) are discussed in more detail.

Gate Driver Guidelines for Use

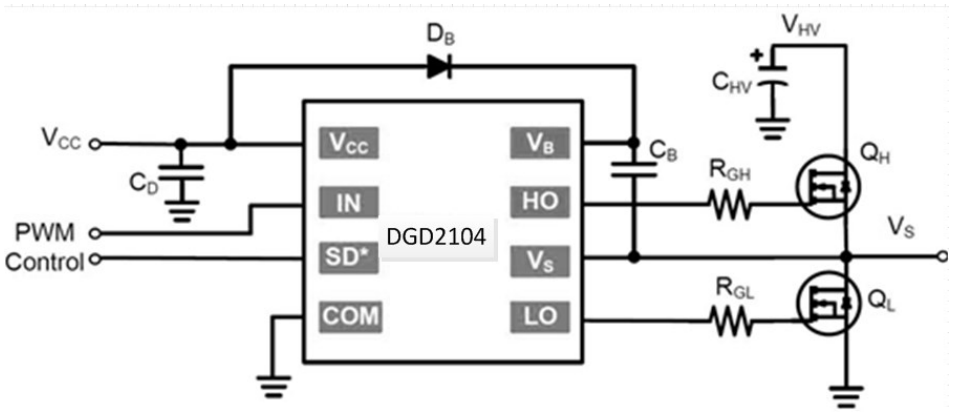

Figure 3: DGD2104 in a Half-Bridge Configuration

The half-bridge is the configuration used in a 3-phase BLDC motor driver. In a half-bridge configuration (see Figure 3) the source of the high-side MOSFET (Q_H) and the drain of the low-side MOSFET (Q_L) are connected. That line (V_S) is both the return for the high-side in the gate driver IC as well as the output of the half-bridge. When Q_H is on and Q_L is off, V_S swings to high voltage, and when Q_H is off and Q_L is on, V_S swings to GND. Hence the output switches from GND to high voltage at the frequency of HIN and LIN and this line drives a transformer for a power supply, or a coil on a motor. In this half-bridge configuration, DC (from battery for

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example) is input to the MOSFETs, and converted to a PWM signal at that DC voltage at V_S (Figure 3). The MOSFETs operate in saturation mode by fully enhancing the channel by providing sufficient gate charge. As it switches, the cycle time needs to be minimized to reduce switching losses as it crosses the linear region from off-state to on-state, and vice versa.

One important function of the gate driver IC in the half-bridge configuration is to convert the logic signals of control (most Diode's Gate Driver ICs operate down to 3.3V), to a voltage level and current capacity to drive the gate of the MOSFET or IGBT; this requires driving large currents initially to turn-on and off the MOSFET quickly by charging and discharging the gate capacitance. Also, the floating well of the high-side allows high voltage operation in the bootstrap operation.

Diode's gate driver IC's are designed for bootstrap operations to drive the high-side power devices. The bootstrap capacitor has to be properly charged per cycle in order for the circuit to operate without any anomalies. Consequently, this simple and inexpensive method comes with limitations. This section discusses the selection of bootstrap components to aid engineers in properly designing their power systems.

Bootstrap Capacitor Selection

The bootstrap capacitor C_B in Figure 3 provides the supply for the high-side drivers. Bootstrap capacitors are often ceramic for the low ESR performance; motors are noisy environments, and a low inductance path from capacitor to high-side will allow the capacitor to supply the charge faster, minimizing spiking. Also the bootstrap capacitor must be adjacent to the V_B and V_S pin on the IC. Generally bootstrap capacitors fall in the range of 0.47µF to 10µF or more, depending on the need in the application. In a motor application, starting with a bootstrap capacitor of 1µF or 2.2µF can be a good starting place. If V_{BS} dips during the on-time, then a larger capacitor is required to supply the charge. Also for voltage ratings consider V_S undershoot which will increase V_{BS}, hence for a 15V operation, a 50V capacitor is a good choice. Also if space allows, a low value and high value capacitor is a good choice to provide charge for the fast transient and then the longer on cycle; for example a 1µF in parallel with a 0.1µF.

Bootstrap Diode Selection

The chosen bootstrap diode should be rated higher than the maximum rail voltage since the diode must be able to block the full rail voltage and any spikes seen at the Vs node. The diode's current rating is simply the product of total charge (Q_T) required by the HVIC and the switching frequency. An ultrafast recovery diode is recommended to minimize the reverse recovery current.

VS Undershoot and Improving Under-shoot and Noise Performance

Power applications with half-bridge topologies typically drive an inductive load, for example transformer or motor, and often switch large currents at high voltages at high speed. This creates an environment of high dV/dt and high dI/dt, increasing susceptibility to parasitic elements; one well known problem is V_S undershoot.

Considering the circuit in Figure.4; when Q_H is on and V_S is at high voltage, load current (I_L) drives the inductive load; but when Q_H turns off the current through the inductive load will not change instantaneously so a current is formed through the free-wheeling diode of the low-side, I_{FW}. The voltage drop of the diode will cause a $-V_S$ occurrence. Other contributions to dynamic V_S undershoot are the spikes caused from the high dI/dt through the parasitic inductances, L_{P1} and L_{P2}, which are in the power switching path. Hence the amplitude of the V_S undershoot will be proportional to the parasitic inductances L_{P1} and L_{P2}, the turn-off speed, and the dI/dt of the switching device.

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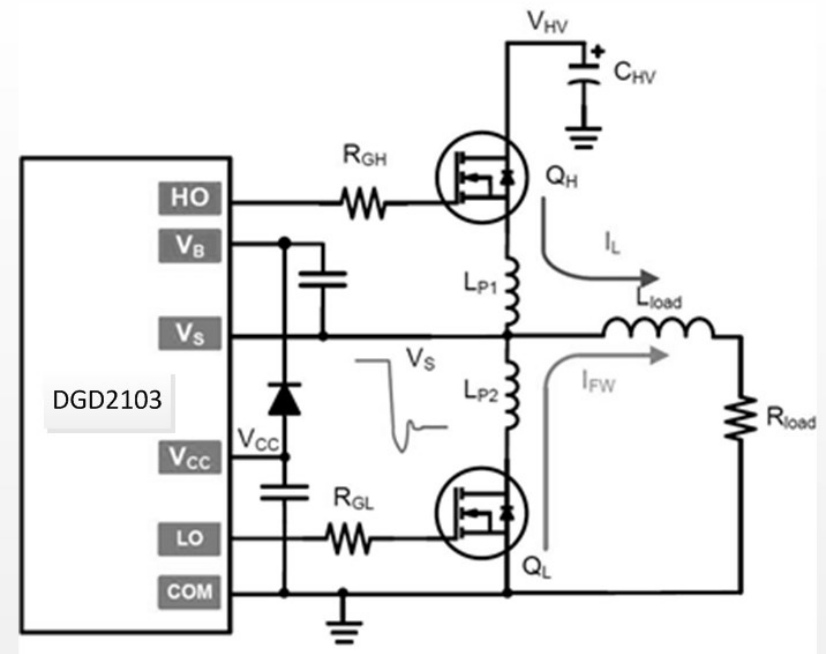

Figure 4: V_S Undershoot Phenomenon

The danger of V_S undershoot is that, an undershoot of less than -5V, then the DGD2103 will function as expected. But if the undershoot is greater than about -5V, but less than the absolute maximum rating of V_S (V_B – 24V), then the high-side may latch in its position and not switch with a changing input. And of course if V_S undershoot is greater than the absolute maximum ratings the device could be damaged. Also with V_S undershoot, V_B-V_S is increased, and if V_S settles to a static, small, negative voltage, then the bootstrap cap will continue charging. There is danger of overcharging the bootstrap capacitor and having a V_B-V_S greater than the absolute maximum ratings and damage the device.

To improve the V_S undershoot, and overall noise performance:

1) Minimize the parasitic inductances by **improving the layout** of the AC power switching traces. Most importantly ensure the trace of L_{P1} and L_{P2} are wide; it is best to use a fill on top and bottom layer with significant density of through-hole vias. See the layout section to find more detail about optimal layout.

2) Decrease dV/dt and hence decreasing dI/dt by slowing down turn off of the MOSFET. A common way of slowing the power switching element is **increasing the value of the gate resistor (R_{GH} and R_{GL})**. The gate resistor and C_{ISS} of the MOSFET form a low pass filter slowing down the rise and fall time. Other ways to slow down turn-off would be to put a reverse voltage diode with a resistor in series on the gate, parallel with the gate resistor and adding a bootstrap resistor. These points are discussed further more in the next section.

Selecting Gate Resistor

Parasitic inductance along the high current path as described above can cause undesirable V_S undershoot but other parasitic elements can also cause ringing in the V_S line, the gate drive (HO and LO), and on V_{CC}. Of primary importance is to follow good layout guidelines minimizing the gate driver IC to MOSFET distance, minimizing the distance between the MOSFETs, and ensuring the bootstrap and decoupling capacitors are low ESR caps placed close to the IC.

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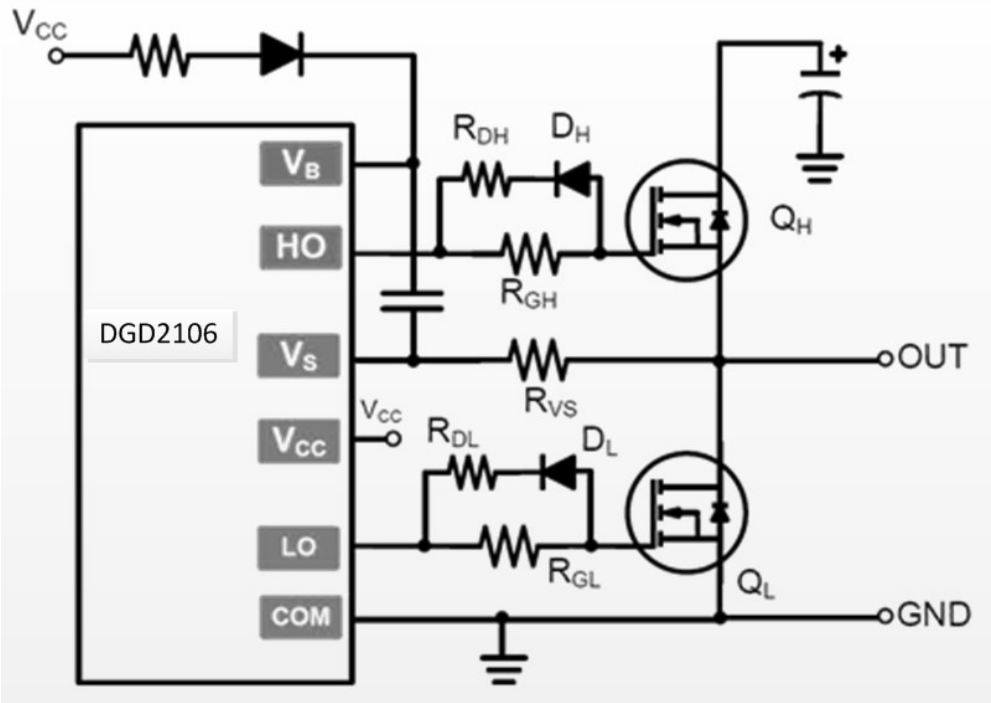

Figure 5: Selecting Gate Resistor and Gate Diode

If further reductions of V_S undershoot, noise and other parasitic ringing are needed, then increasing the gate resistance (R_{GH} and R_{GL} in Figure.5) will slow the turn-on and turn-off time, lowering the dV/dt, and hence lowering the dI/dt, so the ringing can be reduced. Generally, values of gate resistor of 0Ω to 5Ω will have very little effect on the rise and fall time, but increasing the value to 20Ω to 50Ω will have a more considerable effect on rise and fall time, lowering V_S undershoot and reducing noise and parasitic ringing. But increasing the gate resistance has a direct effect of decreasing efficiency; the MOSFET functions in the linear range on turn-on and turn-off, and hence during this time the switching losses are greatest. Hence the choice of gate resistor will be a compromise between parasitic ringing and efficiency.

Other circuit additions can have a positive effect on ringing and general stability mostly by increasing turn-on and turn-off of the MOSFET by shaping (delaying) the gate drive signal. A resistor in series with V_S to OUT (R_{VS}) will have a limiting of turn-on and turn-off for the high-side only. The current path to provide the charge to the MOSFET gate capacitance (HO on), from V_B, and the current path to discharge the MOSFET gate capacitance (HO off) both flow through R_{VS}. A diode (D_L and D_H) that is positive biased during turn-off of the gate drive can be used to separately control turn-on and turn-off times. Adding a resistor in series with the diode (R_{DH} and R_{DL}) will have the effect of increasing turn-off but not affecting turn-on as the diode is reversed biased and no current will flow (the value of R_{DH} and R_{DL} should be less than RGH and RGL to have a greater effect on turn-off).

Choosing which Diode's HV Gate Driver for a Particular MOSFET/IGBT?

The designer will choose a particular MOSFET or IGBT by simulating (or calculating) average and peak current through the switching devices. When the MOSFET or IGBT is known, next step is choosing the appropriate gate driver IC for the job; the most important parameter to consider in this choice is the gate driver sink/source current. The sink/source current (IO+/IO-) of the device is the device ability to provide a short pulse to the gate of the MOSFET or IGBT. It is important to choose enough current capacity, if current sink/source is too low for the job, then the rise/fall time will be longer, with greater power dissipation losses. But a too large sink/source current may have a too faster rise and fall time causing parasitic problems, and can be too expensive for the job.

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To better match the gate driver IC with the MOSFET, a rule of thumb calculation can be used:

$$I = Q_g / t$$

Q_g = total charge of the MOSFET or IGBT as provided by the datasheet
I = sink/source capability of the gate driver IC
t = rise/fall of the MOSFET

The total charge and rise/fall time of the MOSFET are provided in the datasheet specifications, but possibly tested under different conditions from the application. Therefore the measured value of sink/source current is only a rule of thumb and the possible choice will be from ½ to 2x that calculation. Other factors to consider are frequency of operation and gate resistor value (a large gate resistor value will slow down rise/fall). To give an example, the DMN10H099SK3 (100V 17A) MOSFET is used. From the datasheet,

To achieve a t_r = 50ns, t_f = 50ns, using the datasheet value for Q_g = 25.2nC
I_{source} = 0.5A, I_{sink} = 0.5A

Consequently, the DGD2103, half-bridge Gate Driver, with I_{source} = 0.29A, I_{sink} = 0.6A would be a good match for this MOSFET.

Layout Guidelines

Layout also plays a considerable role since unwanted noise coupling; unpredicted glitches and abnormal operation could arise due to poor layout of the associated components. Figure 6 shows the schematic with parasitic inductances in the high current path (L_{P1}, L_{P2}, L_{P3}, L_{P4}) which would be caused by inductance in the metal of the trace. Considering Figure 6, the length of the tracks in red should be minimized, and the bootstrap capacitor (C_B) and the decoupling capacitor (C_D) should be placed as close to the IC as possible as well as using low ESR ceramic capacitors. And finally the gate resistors (R_{GH} and R_{GL}) and the sense resistor (R_S) should be surface mount devices. These suggestions will reduce the parasitic elements due to the PCB traces.

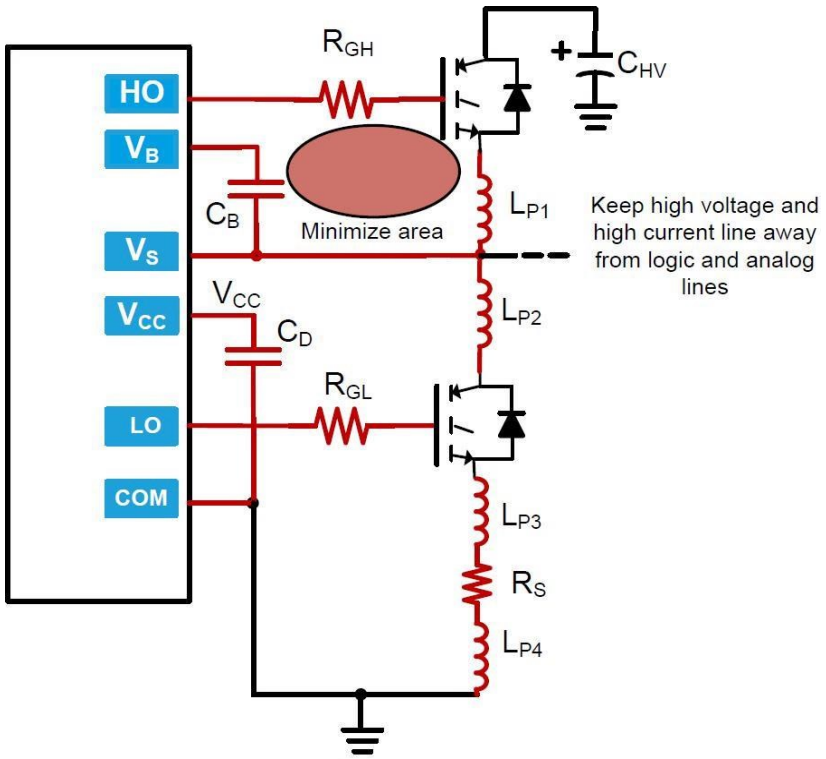

Figure 6: Layout suggestions for single phase of three phase system

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The layout example is seen in Figure 7, where the bootstrap capacitors, C_{B1} and C_{B2}, are placed as close as possible to the HVIC. Ideally, it should be placed immediately over the V_B and V_S pins, however, due to limitations of space, and or desired to have them on the top layer resulted in the next best locations. In addition there is parasitic inductance due to wire bonds inside the IC but this cannot be minimized in the applications.

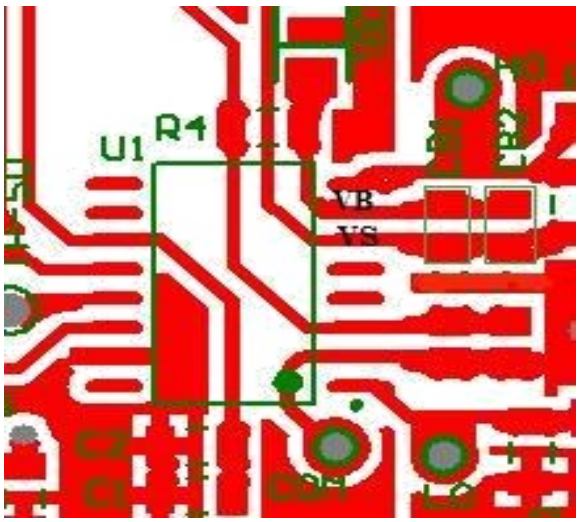

Figure 7: Layout example of bootstrap capacitors in relations to the HVIC

If the bootstrap capacitors were placed without much consideration to the distance from the IC, inefficiencies of the overall system could result as a result of insufficient drive current as required by the load by a certain time. Furthermore, voltage drop seen at the V_{BS} pins could exceed the UVLO protection circuit, causing unwanted shutdown.

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