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Enabling Serial Connectivity

Application Note 325

Design Guide for DisplayPort™ Source Application
PI3EQXDP1201

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AN325

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1. Introduction

This application note covers PI3EQXDP1201 in DisplayPort™ 1.1a & 1.2 source PC applications. Application block diagram, reference schematic, pin control/configuration guideline and PCB layout guideline are included.
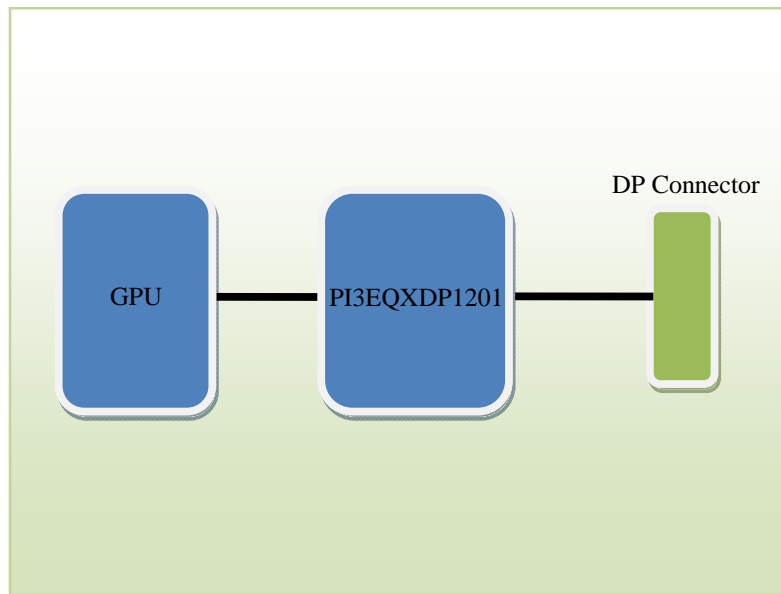

Figure 1: Application Block Diagram

GPU may have combined or separated AUX and DDC output, and the PI3EQXDP1201 re-driver may be used in Single (+3.3V only) and Dual (+3.3V and +1.5V) power supply mode. As a result, four corresponding application schematics are included in this document to cover all these applications as below:

1. Dual Power Supply Mode for source application with separated AUX and DDC output
2. Dual Power Supply Mode for source application with combined AUX and DDC output
3. Single Power Supply Mode for source application with separated AUX and DDC output
4. Single Power Supply Mode for source application with combined AUX and DDC output

2. Reference Schematics

Dual Power Supply Mode for source application with separated AUX and DDC output
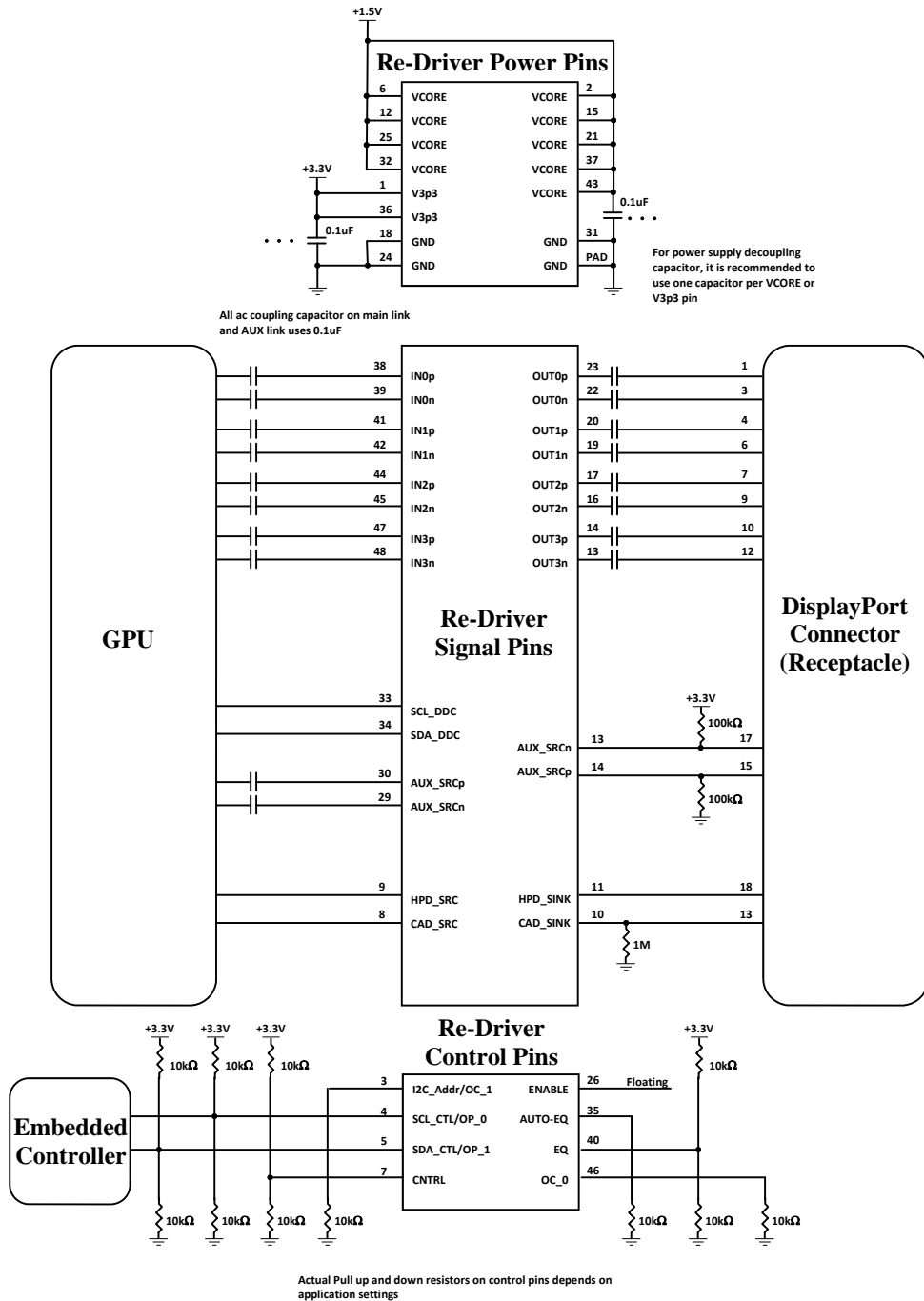
Figure 2: Application Schematic, PI3EQXDP1201ZBE Dual Power Supply Mode for source application with separated AUX and DDC output

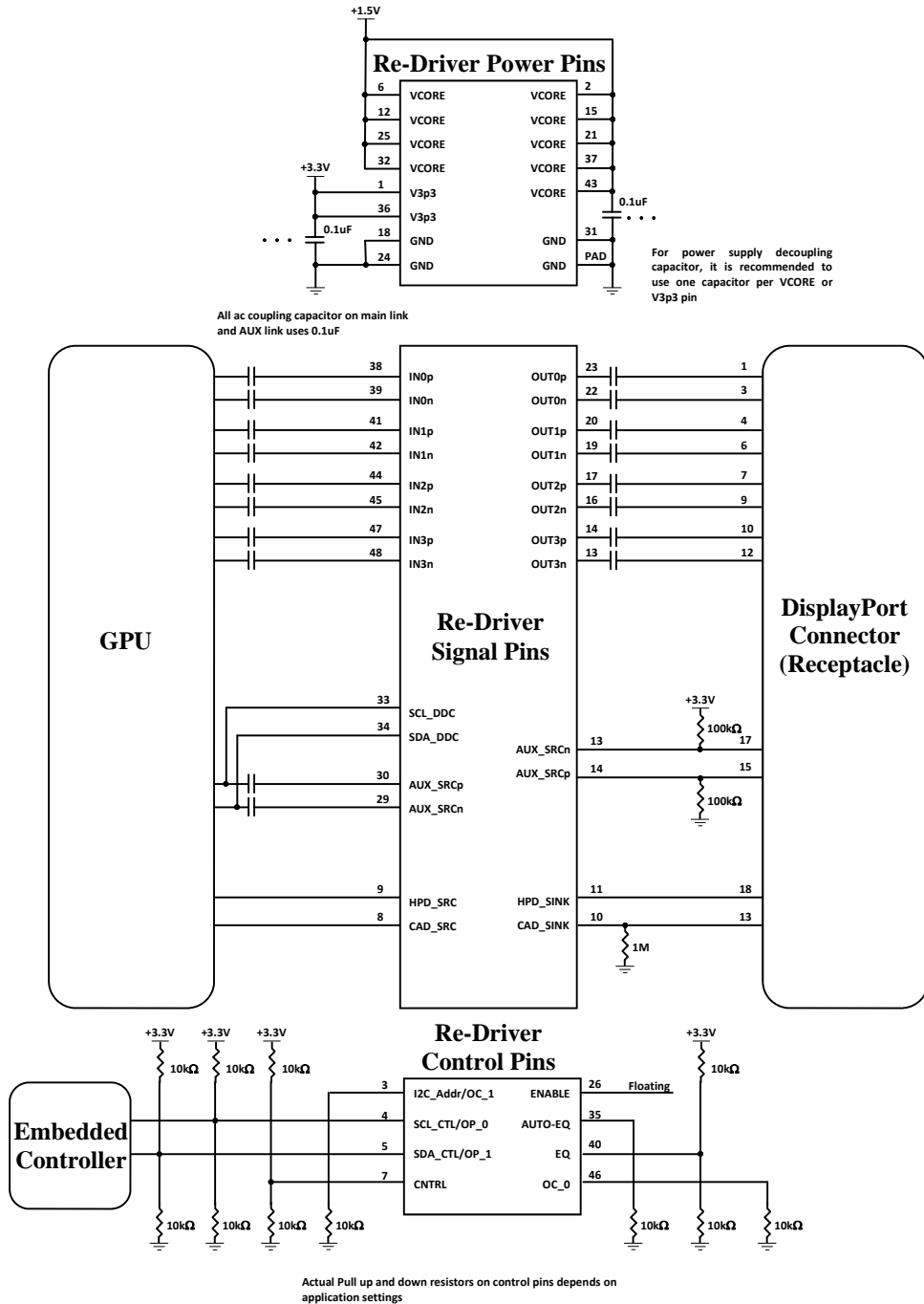## Dual Power Supply Mode for source application with combined AUX and DDC output

Figure 3: Application Schematic, PI3EQXDP1201ZBE Dual Power Supply Mode for source application with combined AUX and DDC output

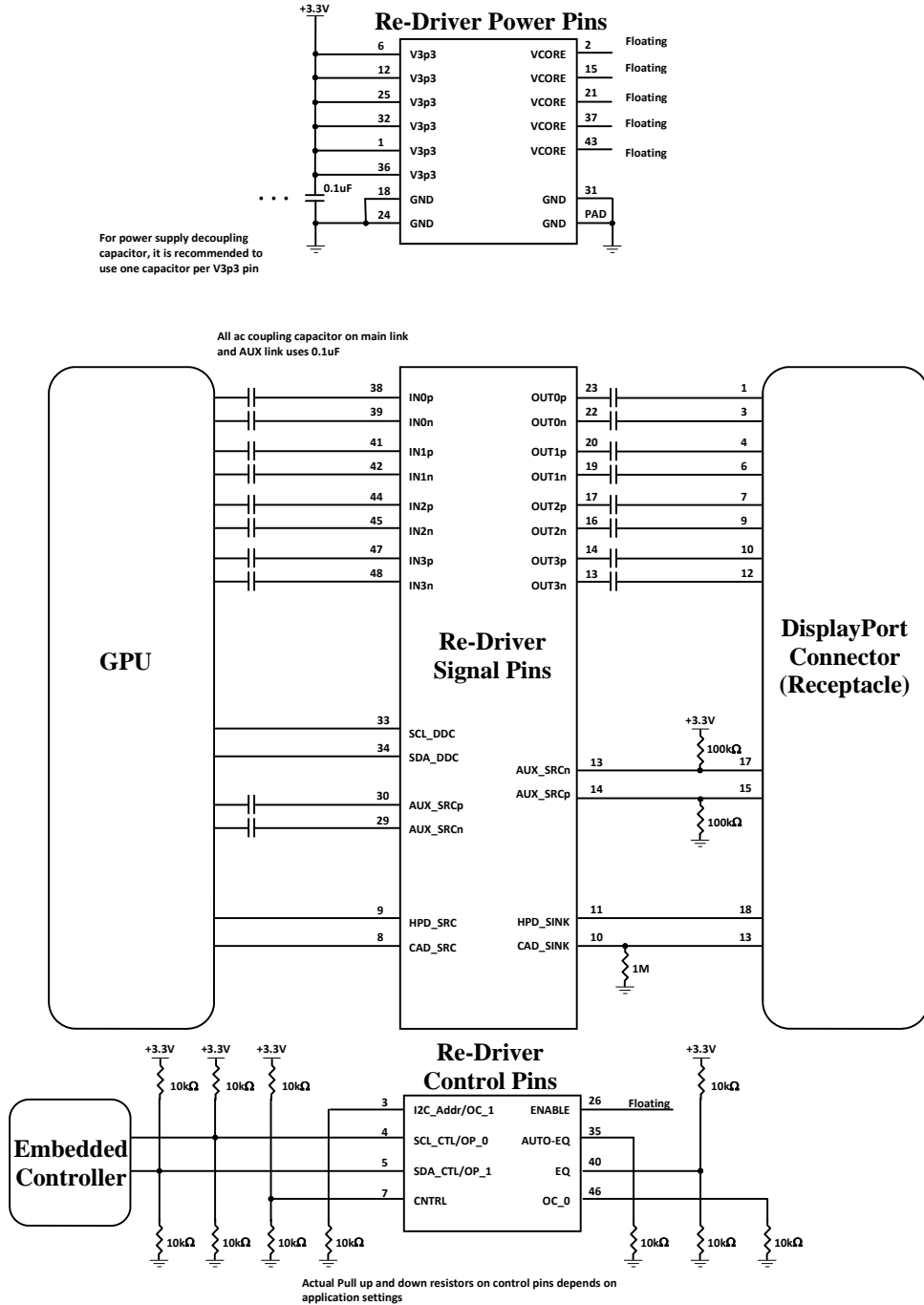## Single Power Supply Mode for source application with separated AUX and DDC output

Figure 4: Application Schematic, PI3EQXDP1201ZBE Single Power Supply Mode for source application with separated AUX and DDC output

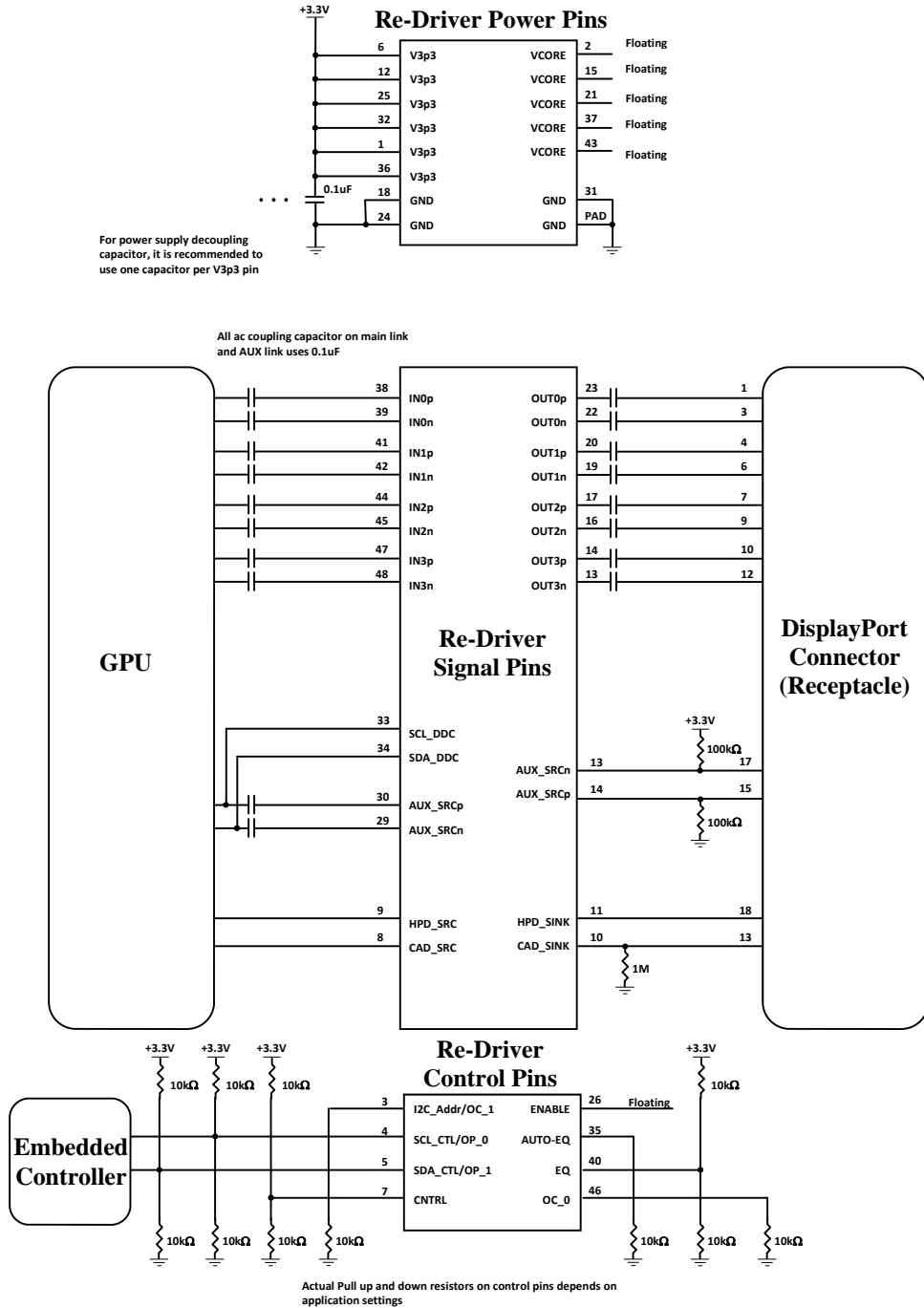## Single Power Supply Mode for source application with combined AUX and DDC output

Figure 5: Application Schematic, PI3EQXDP1201ZBE Single Power Supply Mode for source application with combined AUX and DDC output

3. Pin Control and Configuration Guideline (Pin Control Mode for ZB48 package)

Input Control

EQ Control
PCB trace loss is proportional to frequency and length of PCB trace. Equalizer is used to compensate the input trace loss in order to obtain a better eye opening; hence appropriate equalizer gain should be used. To determine how much equalizer gain is needed, we need to know the PCB trace loss.

To consider appropriate EQ setting on our applications, the pre-emphasis level from the GPU output is also needed to be considered as overall boost, overall boost is used to compensate the overall trace loss.

Overall Boost (dB) = Pre-emphasis (dB) + EQ (dB)

Pre-emphasis = Output pre-emphasis setting on GPU
EQ = Input EQ setting of our PI3EQXDP1201

For example, if the trace length from GPU to our PI3EQXDP1201 is 18 inches and assumes that there is no other parts in between to generate extra loss, the trace loss from Table 1 is about 3dB at 1.25GHz which is about 2.5Gbps data rate and it is closed to DP HBR 2.7Gbps.

	PCB insertion loss (dB)				
	0.825GHz	1.25GHz	2.475GHz	4.125GHz	5.1GHz
3.9 inch	-0.53	-0.75	-1.21	-1.86	-2.25
6.0 inch	-0.78	-1.06	-1.83	-2.84	-3.44
12 inch	-1.47	-2.02	-3.64	-5.51	-6.82
18 inch	-2.15	-2.99	-5.22	-8.07	-8.82
24 inch	-2.89	-4.04	-7.03	-11.00	-13.18

Table 1, measured insertion loss of our FR-4 PCB Trace Card (W/S=9/11, 100ohm differential trace)
Remark: This PCB trace loss is only for reference, for different trace design trace loss will be different

To compensate this 3dB PCB trace loss, EQ setting at 3dB can be chosen if we assume 0dB pre-emphasis is being used. Hence, we can set EQ=L & Auto EQ=L if Fixed EQ mode is used; or, we can set EQ=L & Auto EQ=H if Auto EQ mode is used.

Our Re-Driver Input EQ settings can be configured as two EQ modes, which is **Auto EQ mode** (Auto EQ=H) and **Fixed EQ mode** (Auto EQ=L). In Fixed EQ mode, the EQ value is as below Table 2.

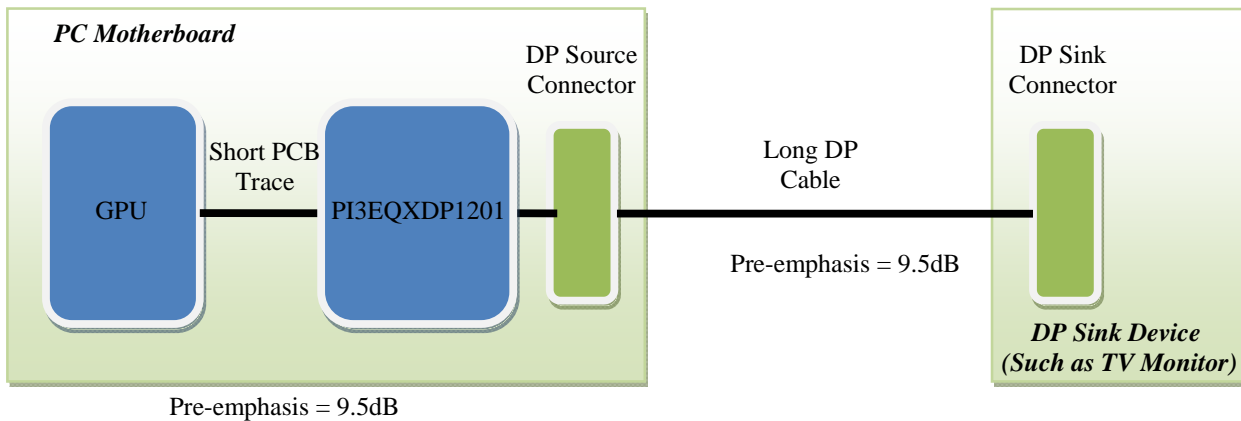| EQ, Pin 40	Auto EQ, pin 35	EQ Value @ 5.4Gbps
L	L	3dB
M	L	6dB
H	L	9dB

Table 2, EQ value in Fixed EQ mode

Another EQ mode is Auto EQ mode, EQ value at this mode is varying with Pre-emphasis setting .There are three Auto EQ modes which can be selected by the following Table 3.

EQ, Pin 40	Auto EQ, Pin 35	Auto EQ mode	EQ Value at each Pre-emphasis setting			
			0dB	3.5dB	6dB	9.5dB
L	H	Mode 0	3dB	0dB	-1dB	-2dB
M	H	Mode 1	6dB	3dB	0dB	-1dB
H	H	Mode 2	9dB	6dB	3dB	0dB

Table 3, EQ value in Auto EQ mode

Auto EQ feature is designed to achieve optimal equalization at different application situations. Figure 6 is an example, there is short PCB trace (less insertion loss) on DP source device routing from GPU to our re-driver input and there is long DP cable (more insertion loss) connecting between DP source device & DP Sink Device. During DP link training, DP source device is trying to increase the pre-emphasis to compensate the long DP cable loss; however, high pre-emphasis setting will make our re-driver input being over equalized due to smaller insertion loss on the short PCB trace. For this reason, our Auto EQ feature is designed to deal with this situation.

Using same example in Figure 6, if 6dB EQ is needed to compensate the PCB trace loss and fixed EQ mode is used with pre-emphasis 9.5dB, then overall boost is 6dB + 9.5dB = 15.5dB; if Auto EQ mode is used, then overall boost will be reduced to -1dB + 9.5dB = 8.5dB. Hence, Auto EQ mode is used to avoid **over equalization** in this application scenario.

PC Motherboard

DP Source Connector

DP Sink Connector

GPU — Short PCB Trace — PI3EQXDP1201 — Long DP Cable

Pre-emphasis = 9.5dB

DP Sink Device (Such as TV Monitor)

Pre-emphasis = 9.5dB

If Fixed EQ mode EQ 6dB is chosen, overall boost is 6dB + 9.5dB = 15.5dB
If Auto EQ mode 1 is chosen, overall boost is -1dB + 9.5dB = 8.5dB

Figure 6: Auto EQ application example

Output Control

CNTRL = M or floating

Control Pins					Resultant Settings		
CAB_DET	OC_1	OC_0	OP_1	OP_0	Output Swing	Pre-emphasis	AUX Listener
0	1	x	x	0	Follow AUX	Follow AUX	ON: Use DPCD registers
0	1	x	x	1	Follow AUX	Follow AUX, with 1.5dB boost	ON: Use DPCD registers
0	0	0	x	0	800mV	0dB	ON: Override register setting
0	0	1	x	1	600mV	3.5dB with 1.5dB boost	ON: Override register setting
1	x	x	x	0	800mV	0dB	OFF: Not override register setting
1	x	x	x	1	800mV	0dB with 1.5dB boost	OFF: Not override register setting

Table 4, function of output control pins

Control Pins in Table 4 is used to set the re-driver output swing and pre-emphasis. If the re-driver is placed a little bit far away from the DP connector, 1.5dB boost on the pre-emphasis can be chosen on above table settings to compensate the PCB trace loss from re-driver output to DP connector. In DP mode (CAD_DET=0), output Swing and pre-emphasis can be chosen to follow DPCD registers or fixed values. In DP mode fixed output swing and pre-emphasis settings, AUX listener is still ON and listens to the AUX transactions on specific DPCD registers and override into our re-driver registers, but output swing and pre-emphasis will not follow DPCD registers in fixed output swing and pre-emphasis settings.

4. PCB Stackup Information

Below is an example of a 4 layer PCB board stackup and 100ohm differential trace design information, also its associated PCB trace loss. The W/S 9/10 mil is typically for medium PCB board density applications, for high PCB board density, it may use W/S 5/5 mil differential trace which will introduce higher insertion loss. Hence, it is recommended to measure the PCB trace loss on target PCB and then uses this information to select appropriate EQ setting on our re-driver to compensate the input trace loss.

Signal	18um (0.5oz)	PCB thickness $\cong$ 1.6mm
Prepreg 1080 + 3313	2.8mil + 3.8mil	100ohm Differential Trace W/S = **9/10** mil
GND	35um (1oz)	Isolation space = 4 x 6.6mil = 26.4mil
CORE	44.5mil	
PWR	35um (1oz)	
Prepreg 1080 + 3313	2.8mil + 3.8mil	
Signal	18um (0.5oz)	
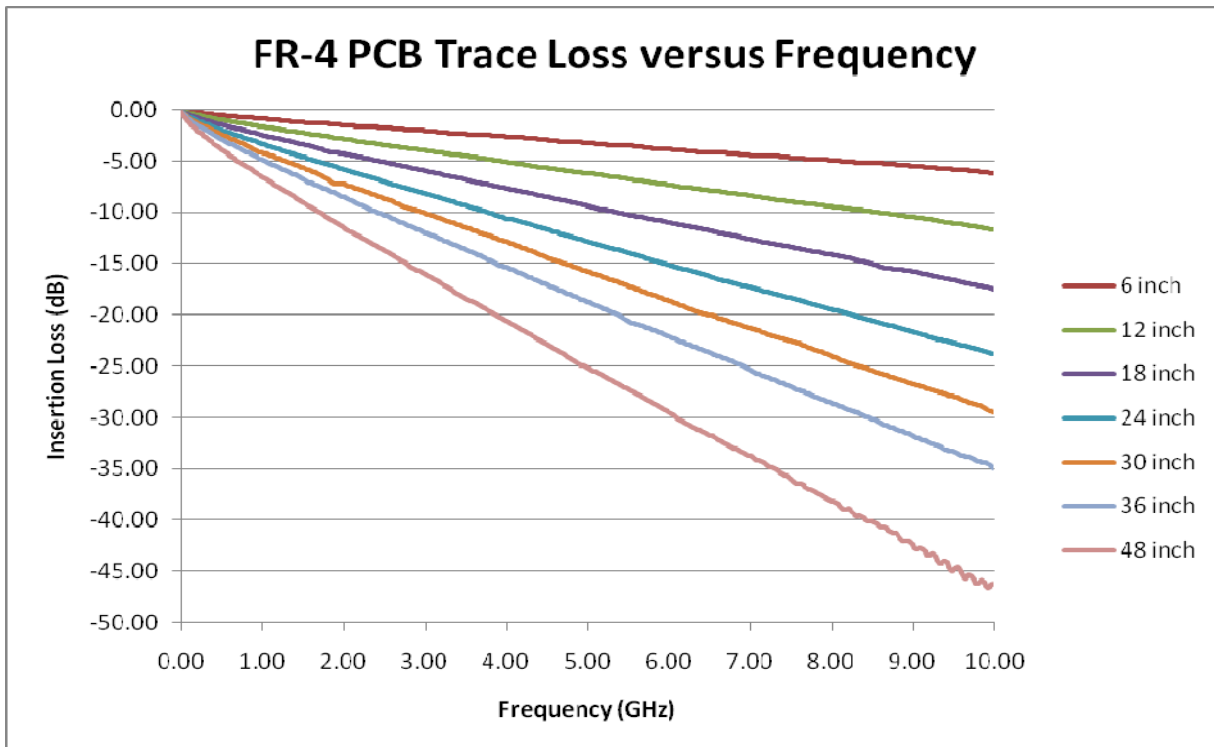
Figure 7: FR-4 PCB Trace Loss versus Frequency

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5. Layout Guideline

Power Supply Decoupling

It is recommended to put **0.1uF** decoupling capacitors on each VDD pins of our part. On top of 0.1uF decoupling capacitors on each VDD pins, it is recommended to put a **10uF** decoupling capacitor for stabilization and Ferrite bead for isolation. Each **0.1uF** decoupling capacitor should be placed as closed as possible to each VDD pin to reduce the trace inductance as in below Figure 7. Decoupling capacitors are placed on the bottom layer for easy implementation and connected to VDD & GND planes through via; each decoupling capacitor should have its own via to VDD & GND planes and via should not be shared with other decoupling capacitors.
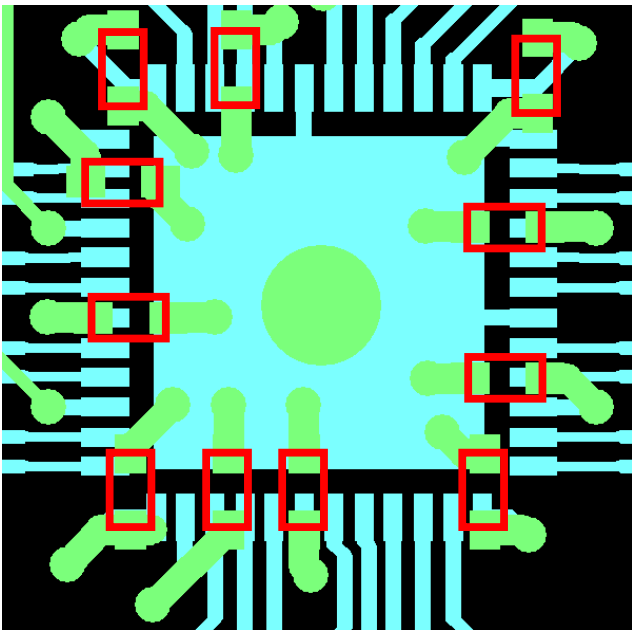

Figure 8: Decoupling capacitors placement

Main Link Differential Trace keeps same trace length

Main Link differential trace should be kept in same length on same lane or inter lanes to minimize the inter-pair or intra-pair skews
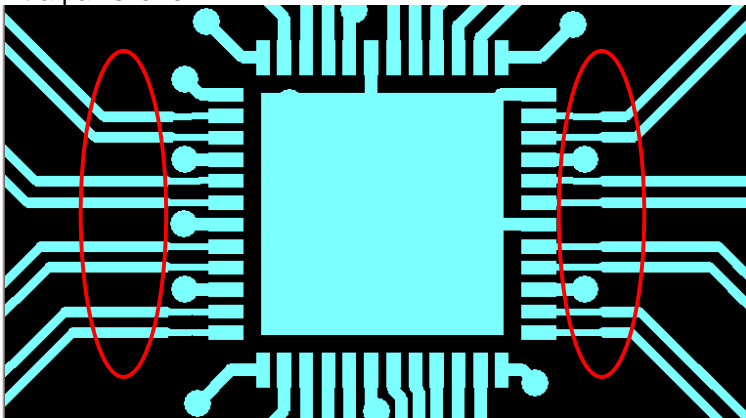

Figure 9: Differential Trace routing

AUX Channel Trace

As the AUX channel is running at 720Mbps in DP1.2 FAUX application; hence, AUX trace routing guideline is provided here to maintain the impedance continuity on AUX channel.

1. AUX Trace should be differential 100ohm
2. 100kohm pull up and pull down resistors on our re-driver AUX_SINKp & AUX_SINKn pins should be routed in this way to minimize the impedance discontinuity
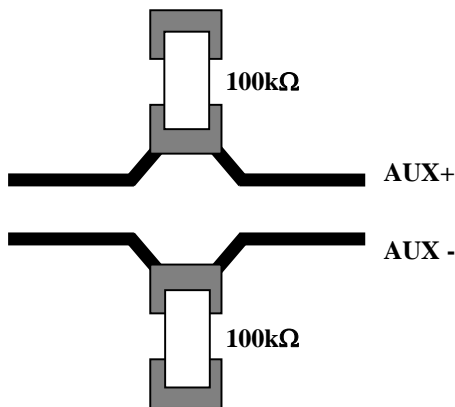

Figure 10: AUX pull up and down resistor layout guideline

3. If AUX and DDC are combined output from GPU, the trace connecting to SCL_DDC & SDA_DDC of our re-driver (yellow highlighted below) should be kept **within 10mm** to minimize the stub effect on AUX trace when operates in DP mode.
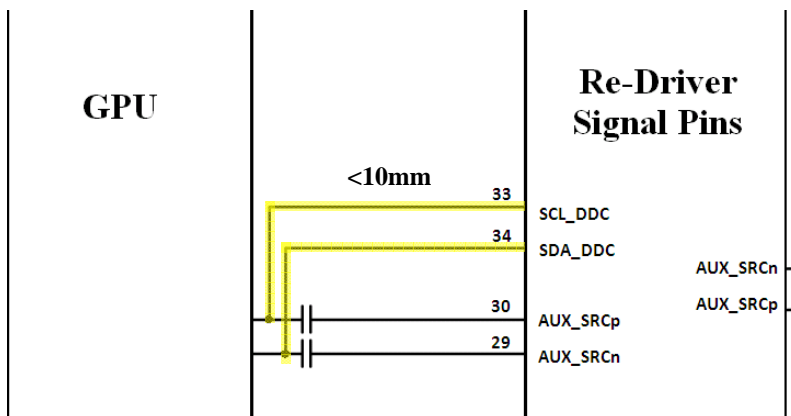

Figure 11: Combined AUX & DDC output to Re-driver layout guideline

Impedance Continuity on high speed trace

(1) Avoid stubs
(2) Avoid trace crossing
(3) Keep adjacent trace gap
(4) Keep Enough grounding
(5) Keep differential impedance within 10%
(6) Keep same trace length
(7) Keep Symmetrical routing
(8) Minimize layer changes on routing or minimize via used

For more details, please refer to our application note "*High Speed PCB Layout Guideline*".

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