PI2EQX6804 and PI2EQX6864
4-lane SAS/SATA ReDriver Application Note

Introduction

Pericom offers two 4-lane SAS/SATA redrivers, which support signals up to 6Gbps: PI2EQX6804-ANJE and PI2EQX6864-AZFE. These devices provide flexible output strength and de-emphasis controls to optimize signals. They pre-compensate for losses across long trace or noisy environment and enable the receiver to receive clean signals with an ideal eye opening.

PI2EQX6804-ANJE provides pin strap and I2C options for output swing/de-emphasis configuration and input equalization, while PI2EQX6864-AZFE provides only I2C option.

Packaging: 100-contact LFBGA (11x11mm) for PI2EQX6804-ANJE
              56-contact TQFN (5x11mm) for PI2EQX6864-AZFE

Main Application:
        Server
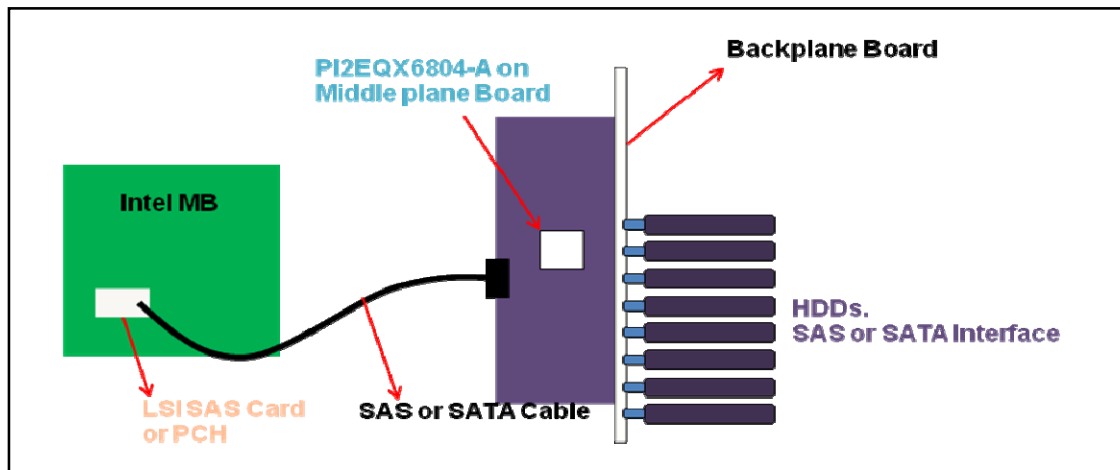   Desktop
        Storage/Workstation

Figure 1: Typical Application Example

Output Swing/De-emphasis and Input Equalization of PI2EQX68x4-A through Pin Strap and I2C Control

PI2EQX6804-A provides two options, outlined below, to configure output swing/de-emphasis and input equalization. PI2EQX6864-A provides only one option - I2C function, which is configured exactly the same way as PI2EQX6804-A.

1. pin-strap function
2. I2C function

The option of the configuration method depends on the state of the MODE pin with 100k internal pull-up resistor.

When MODE pin is set HIGH, all the configuration input pins determine all the configuration settings. Note that all of these control pins have 100k internal PULL-UP resistor, and, therefore, only external pull-down resistors are required. The configuration input pins include: D0_A, D1_A, D2_A, S0_A, S1_A, SEL0_A, SEL1_A, SEL2_A, D0_B, D1_B, D2_B, S0_B, S1_B, SEL0_B, SEL1_B, SEL2_B, DE_A, DE_B, LB# and PD#.

When MODE pin is set LOW, all the internal configuration registers can be programmed by I2C interface. Note that during initial power-on, the value at the configuration input pins are latched to the configuration registers as the initial startup states.

- The integrated I2C interface operates as a slave device, supporting standard rate operation of 100Kbps, with 7-bit addressing mode and LSB indication either a read or write operation as shown below. The address for a specific device is determined by A0, A1 and A4 pins with internal pull-up resistors. So up to eight PI2EQX6804-A devices can be connected to a single I2C bus.

Address Assignment							R/W
A6	A5	A4	A3	A2	A1	A0	R/W
1	1	Program	0	0	Programmable		1=R, 0=W

- Data bytes must be 8-bits long and transferred with MSB first. Please refer to I2C data transfer diagram in Page13 of datasheet. Data byte definition is shown below. Please refer to Page 8 -11 of the datasheet for details.

Configuration Register Summary

Byte	Mnemonic	Function
0	SIG	Signal Detect, indicates valid input signal level
1	RSVD	Reserved for future use
2	LBDEC	Loopback and De-emphasis Control, provides for control of the loopback function and De-emphasis mode (Half-bit or Full-bit)
3	INDIS	Channel Input Disable, controls whether s channels input buffer is enabled or disabled
4	OUTDIS	Channel Output Disable, controls whether a channel output buffer is enabled or disabled.
5	RSVD	Reserved for future use
6	PWR	Power Down Control, enables power down for each channel individually
7	RSVD	Reserved for future use
8	AEOC	A-Channels Equalizer and Output Control
9	BEOC	B-Channels Equalizer and Output Control
10	RSVD	Reserved for future use
11	RSVD	Reserved for future use

- I2C input pins, SCL and SDA, are tolerant with +3.3V power.

- For I2C configuration sequence in details, please refer to Page 6-7 of this document.

External Components Requirement

PI2EQX68x4-A requires AC coupling capacitors for all redriver inputs and outputs. High-quality, low-ESR, X7R, 10nF, 0402-sized capacitors are recommended.

Layout Design Guide

- **Layout Considerations for Differential Pairs**
  - The trace length miss-matching shall be less than 5 mils for the "+" and "–" traces in the same pairs
  - Use wider trace width, with 100ohm differential impedance, to minimize the loss for long routes
  - Target differential Zo of 100ohm ±20%
  - More pair-to-pair spacing for minimal crosstalk coupling, it is recommended to have >3X gap spacing between differential pairs.
  - It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces
  - The use of vias should be avoided if possible, if vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair.
  - Route the differential signals away from other signals and noise sources on the printed circuit board
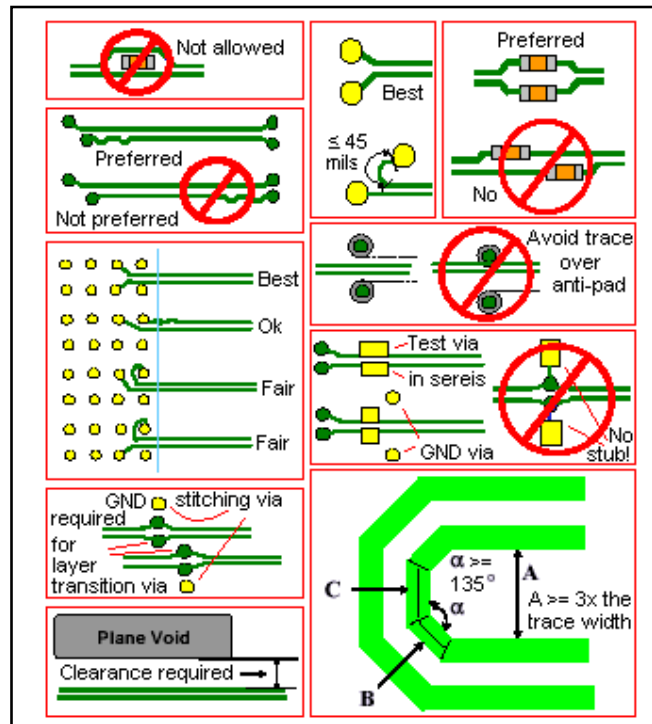
- **PCB Layout Trace Routings**

Figure 2: PCB Layout Trace Routings

Power-Supply bypass

Caution must be taken and details must be carefully observed in high-speed design and to provide a clean power supply. Here are the recommendations:

- The supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The distance to plane should be <50mil.
- The layer thickness of the dielectric should be minimized so that the VDD and GND planes create a low inductance supply with distributed capacitance.
- Be careful to supply bypassing through the proper use of required bypass capacitors. A low-ESR 0.01uF bypass capacitor should be connected to each VDD pin such that the capacitor is placed as close as possible to PI2EQX68x4-A. Smaller body size capacitors can help facilitate proper component placement.
- The distance of capacitors to IC body should be <100mil.
- One capacitor with capacitance in the range of 1uF to 10uF should be incorporated in the power supply bypassing design as well. It is can be either tantalum or an ultra-low ESR ceramic.

Power Supply Sequencing

Proper power supply sequencing is recommended for all devices. Always apply GND and VDD before applying signals, especially if the signal is not current limited.

Caution: Do NOT exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the device.

Equalization Setting

Table 1 below shows various Input Trace and Eye Test with different EQ settings
Figure3 below shows PI2EQX68x4-A test setup for different EQ settings, where R is PI2EQX68x4-A.
Signal Source: PRBS2^7-1 pattern, Differential Voltage is 600mV, Pre-emphasis is 0dB
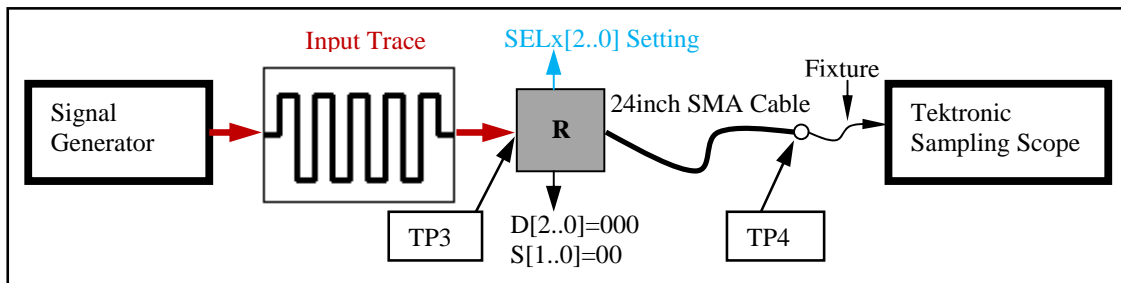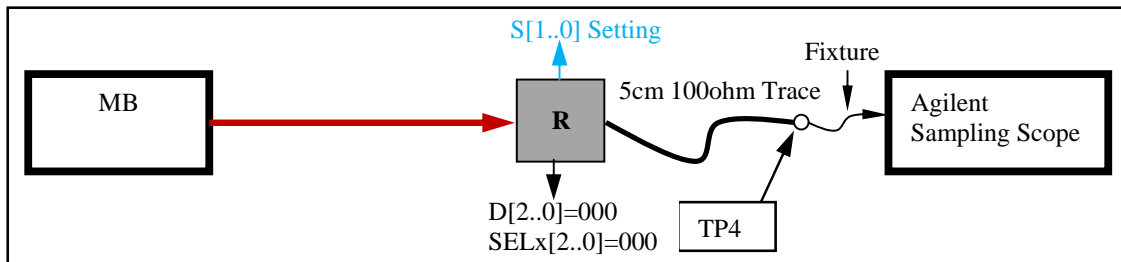

Figure 3: PI2EQX68x4-A test setup for different equalization setting

	Input Trace Length	SEL[2..0] Setting	Input Eye at TP3	Output Eye at TP4
Eye Diagram vs. EQ setting at 6Gb/s	6 inch FR4 Lab trace (-2dB loss at 6GHz)	3.2dB (SEL[2,1,0] =010)		
	18 inch FR4 Lab trace (-6dB loss at 3GHz)	6.9dB (SEL[2,1,0] =100)		
	30 inch FR4 Lab trace (-10dB at 3GHz)	10.4dB (SEL[2,1,0] =110)		
	48 inch FR4 Lab trace (-16dB at 3GHz)	13.8dB (SEL[2,1,0] =111)		

Table 1: Eye Diagram at TP4 vs. Input FR4 trace and EQ setting at 6Gb/s for PI2EQX68x4-A

Output Swing Setting

Figure 4 below shows the PI2EQX68x4-A test setup for different output swing settings, where R is PI2EQX68x4-A.
Signal Source: PRBS2^7-1 pattern, Differential Voltage is 500mV, Pre-emphasis is 0dB

Figure 4: PI2EQX68x4-A test setup for different output swing setting

	S[1..0]=00	S[1..0]=01	S[1..0]=10	S[1..0]=11
Output Swing at TP4 vs. OS setting at 3Gb/s				
Output Swing at TP4 vs. OS setting at 6Gb/s				

Table 2: Output Swing at TP4 vs. OS setting at 3Gb/s and 6Gb/s for PI2EQX68x4-A

De-emphasis Setting

Figure5 is PI2EQX68x4-A test setup for different De-emphasis setting, R is PI2EQX68x4-A.
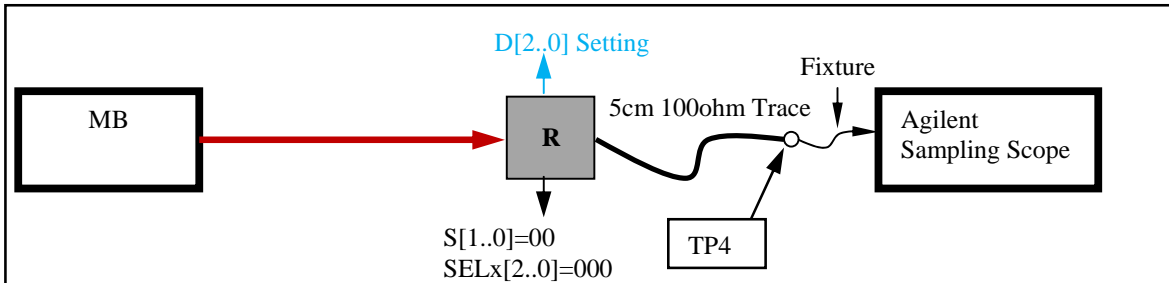Signal Source: PRBS2^7-1 pattern, Differential Voltage is 500mV, Pre-emphasis is 0dB

Figure 5: PI2EQX68x4-A test setup for different De-emphasis setting

	D[2..0]=000	D[2..0]=010	D[2..0]=111
Output De-emphasis at TP4 vs. De-em setting at 3Gb/s			
Output De-emphasis at TP4 vs. De-em setting at 6Gb/s			

Table 3: De-emphasis at TP4 vs. D[2..0] setting at 3Gb/s and 6Gb/s for PI2EQX68x4-A

I2C Configuration Sequence

Note: there is one DUMMY byte to be added into sequence.
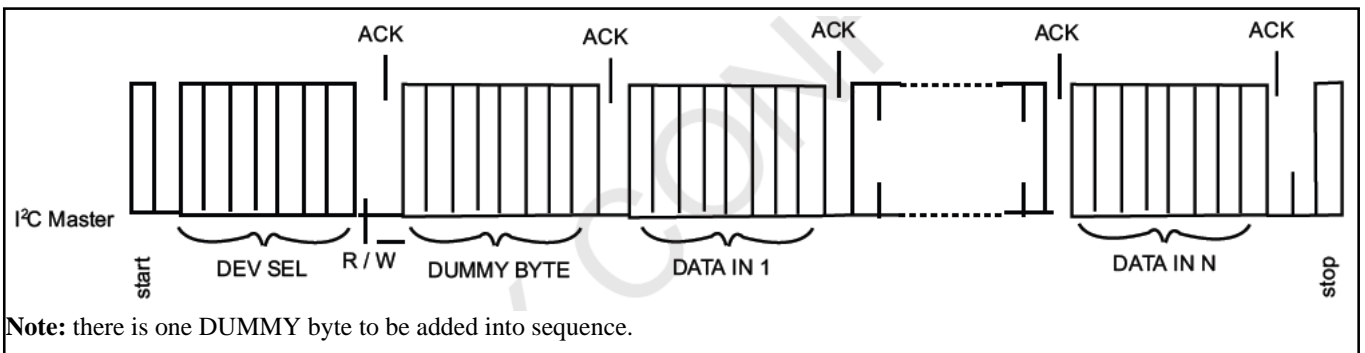
Figure 6: WRITE Sequence Diagram

Figure 7 below is one example for write sequence at Address = C0 (A4, A1, A0 are pulled down) and Data byte[0..11]=00,00,F0,00,00,FF,FF,FF,00,00,00,EF.
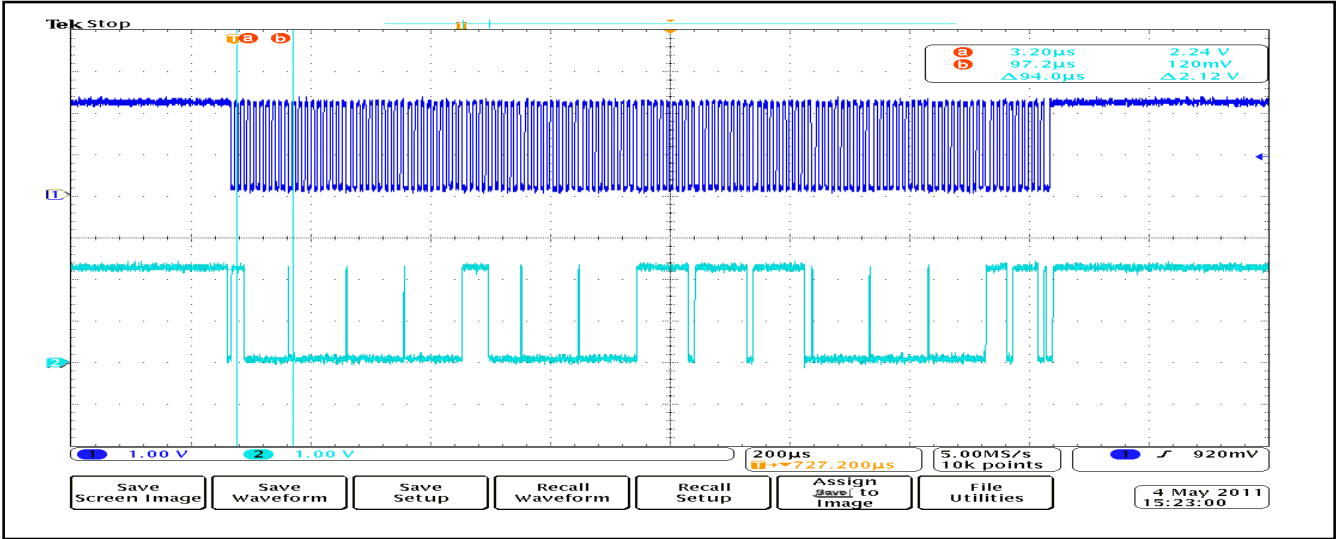

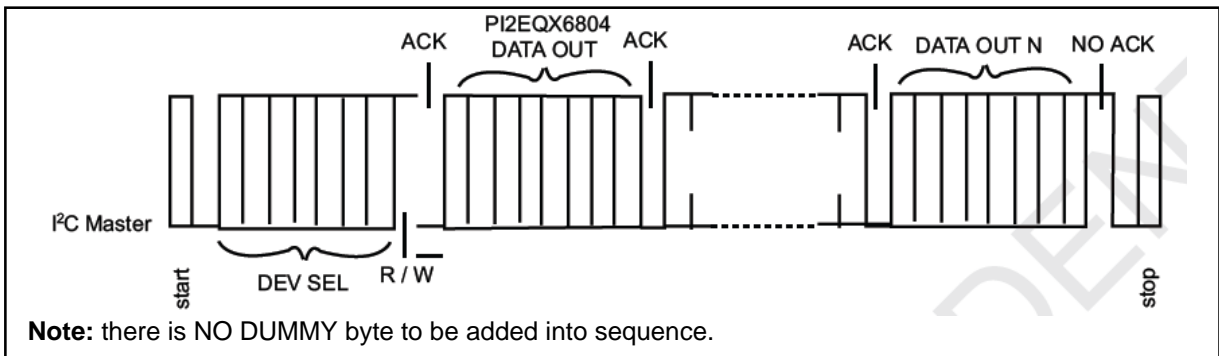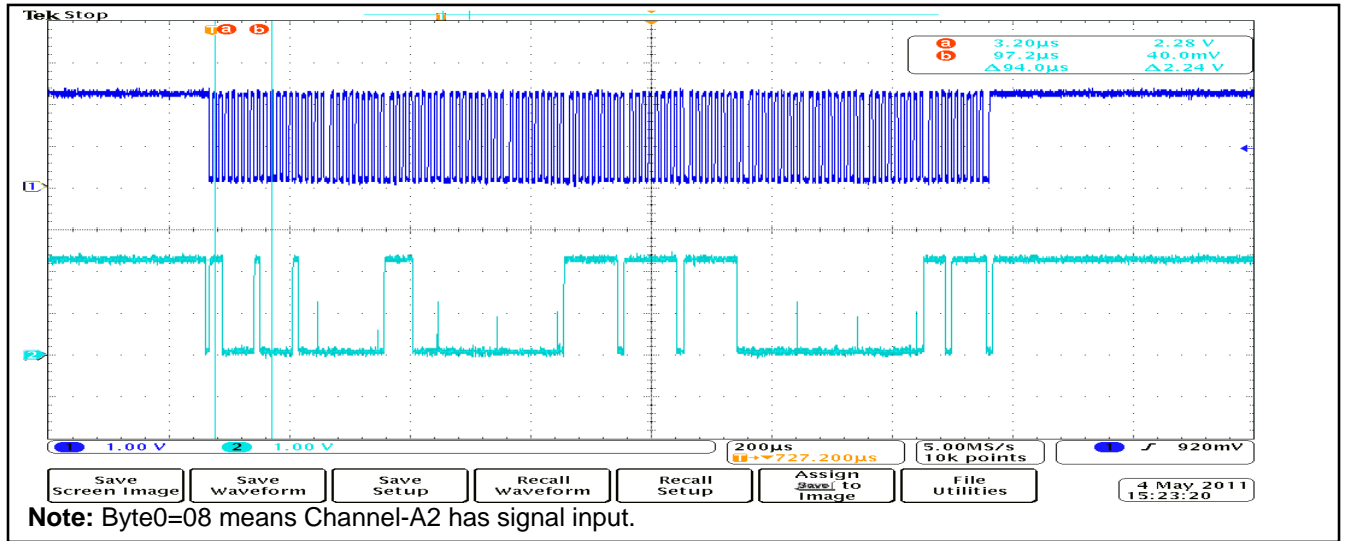**Figure 7: I2C WRITE Sequence Sample**

Note: there is NO DUMMY byte to be added into sequence.

Figure 8: I2C READ Sequence Diagram

Note: Byte0=08 means Channel-A2 has signal input.

Figure 9: I2C READ Sequence Sample

Application Note

Typical Application Circuit

Figure 10 below shows the typical application circuit of PI2EQX6804-A.
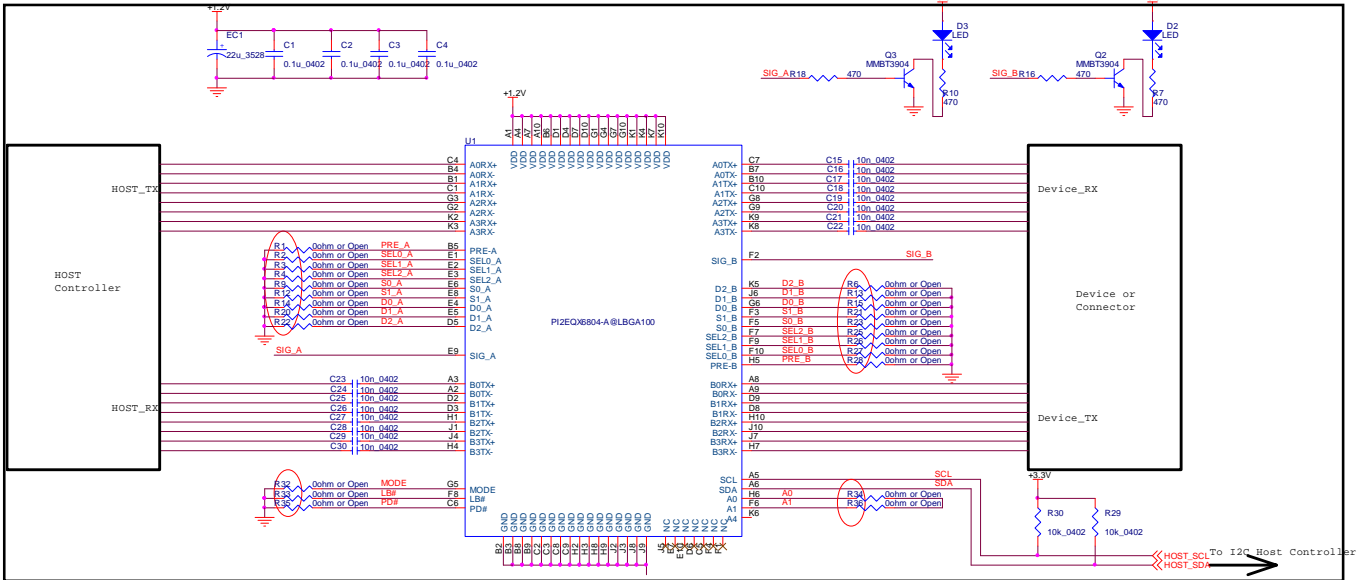
Figure 10: Typical Application Circuit of PI2EQX6804-A

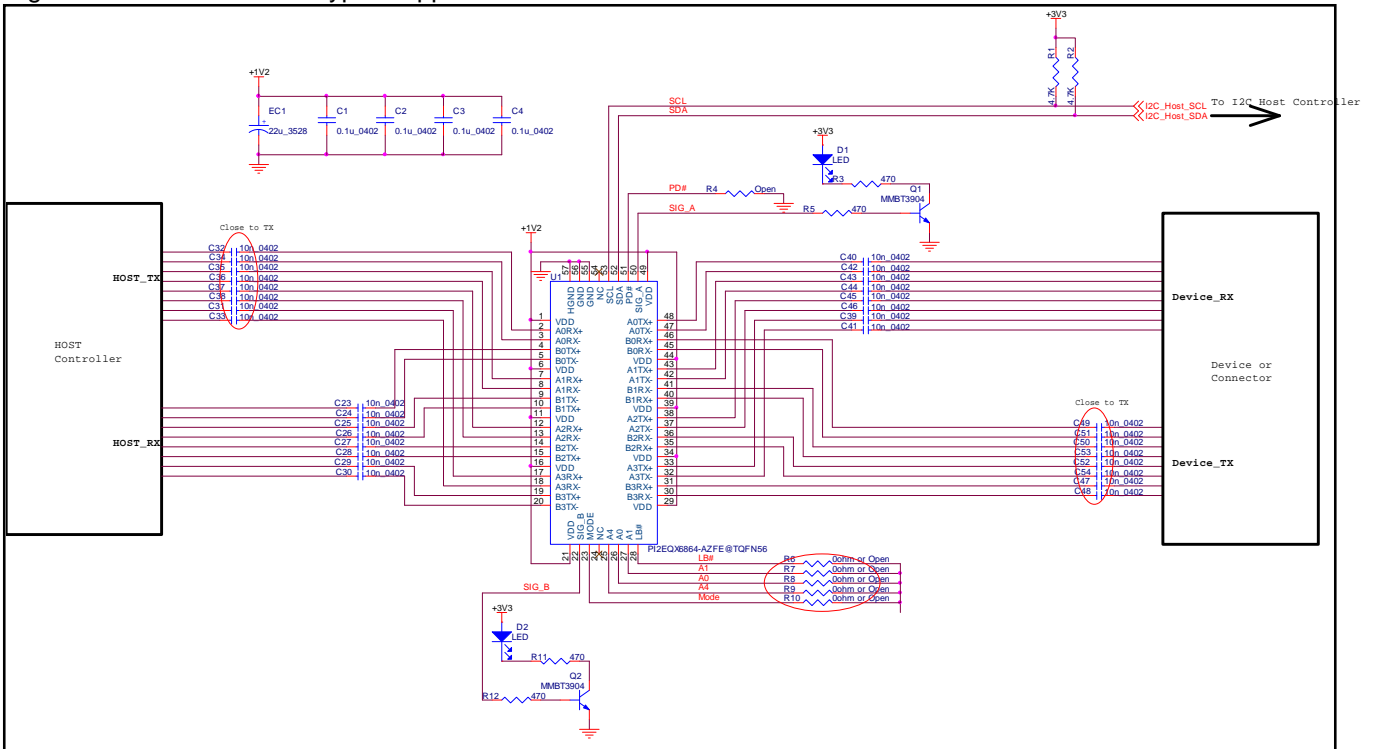Figure 11 below shows the typical application circuit of PI2EQX6864-A.

Figure 11: Typical Application Circuit of PI2EQX6864-A

PCB Layout Sample

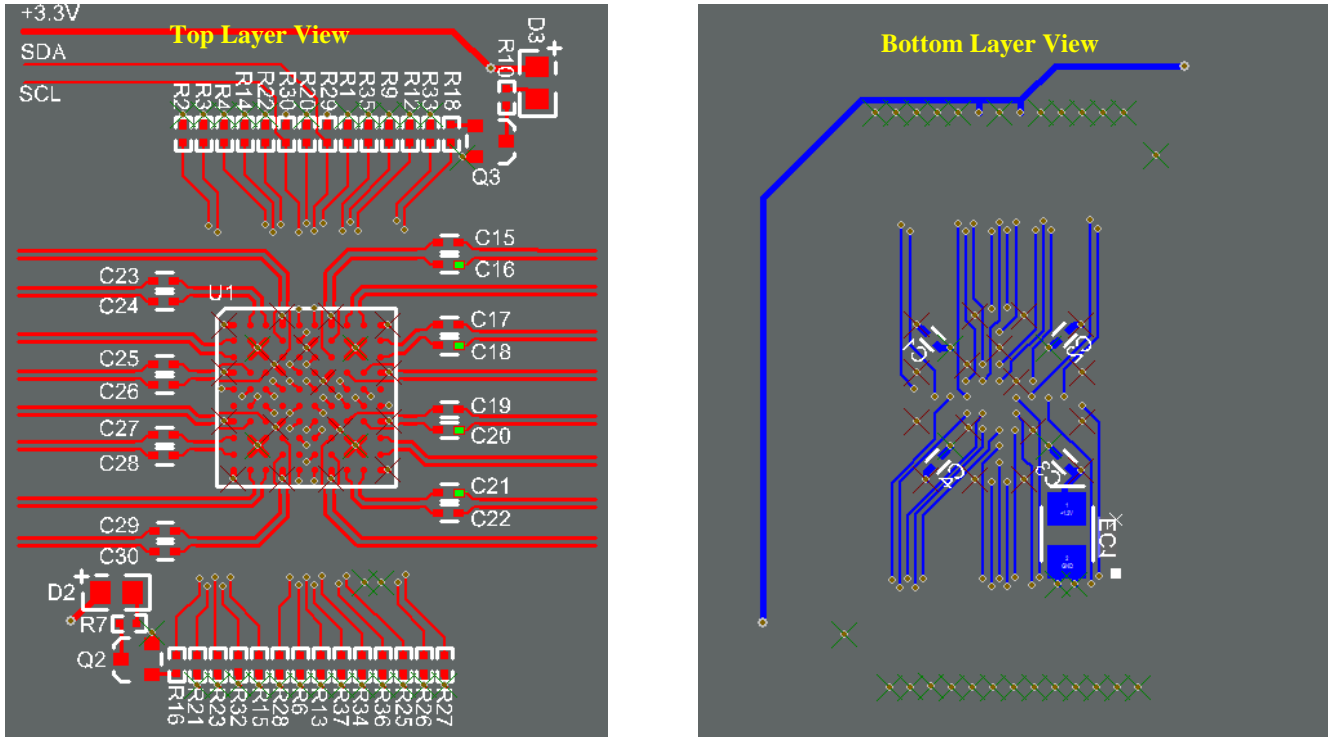Figure12 shows the typical layout routing of PI2EQX6804-A.

Figure 12: Typical Layout Routing of PI2EQX6804-A
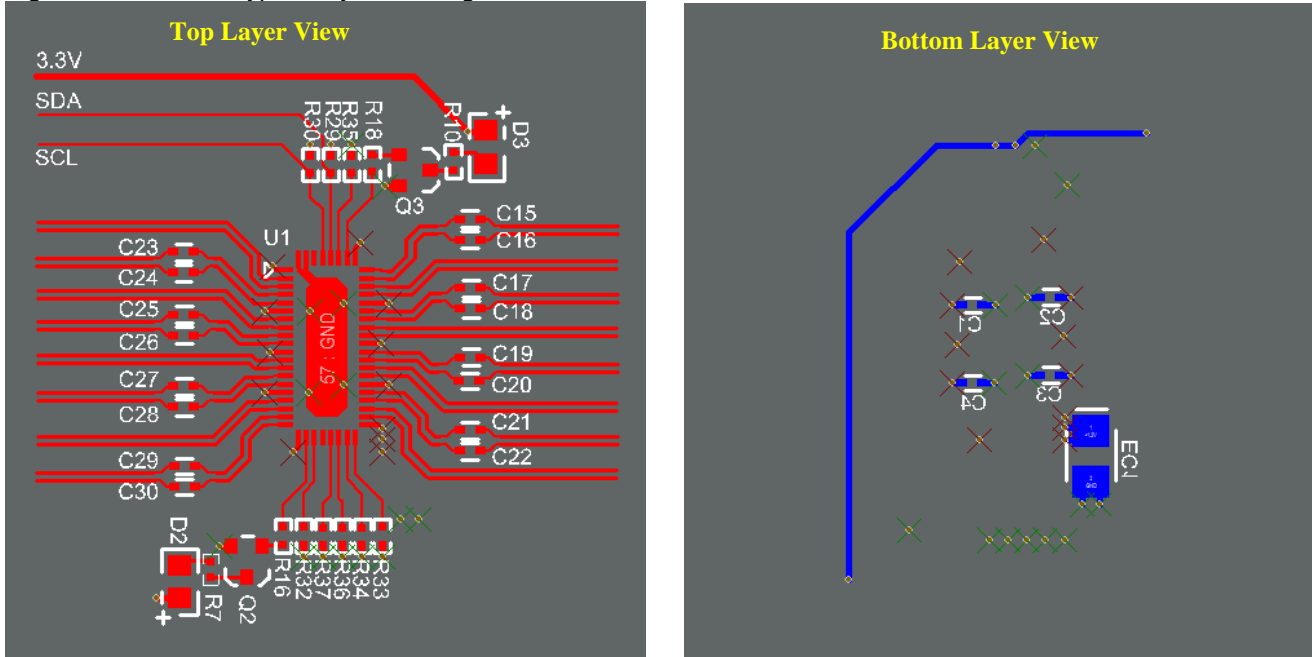
Figure12 shows the typical layout routing of PI2EQX6864-A.

Figure 13: Typical Layout Routing of PI2EQX6864-A