AN1180

DGD05463 DGD0506A Application Note

David Toro, Bipolar Business Unit, Diodes Incorporated

The DIODES™ DGD05463 and DGD0506A high-frequency, half-bridge gate drivers with programmable deadtime are used to optimally drive the gate of MOSFETs. The DGD05463/06A respectively have an integrated bootstrap diode for ease of design and lower BOM. Below (Figure 1) is an example application using the DGD0506A with MOSFETs in a Brushless DC motor driver application. In this discussion, the important parameters needed to design in the DGD05463/06A are discussed; main sections are bootstrap capacitor selection, gate driver component selection, decoupling capacitor discussion and PCB layout suggestions.

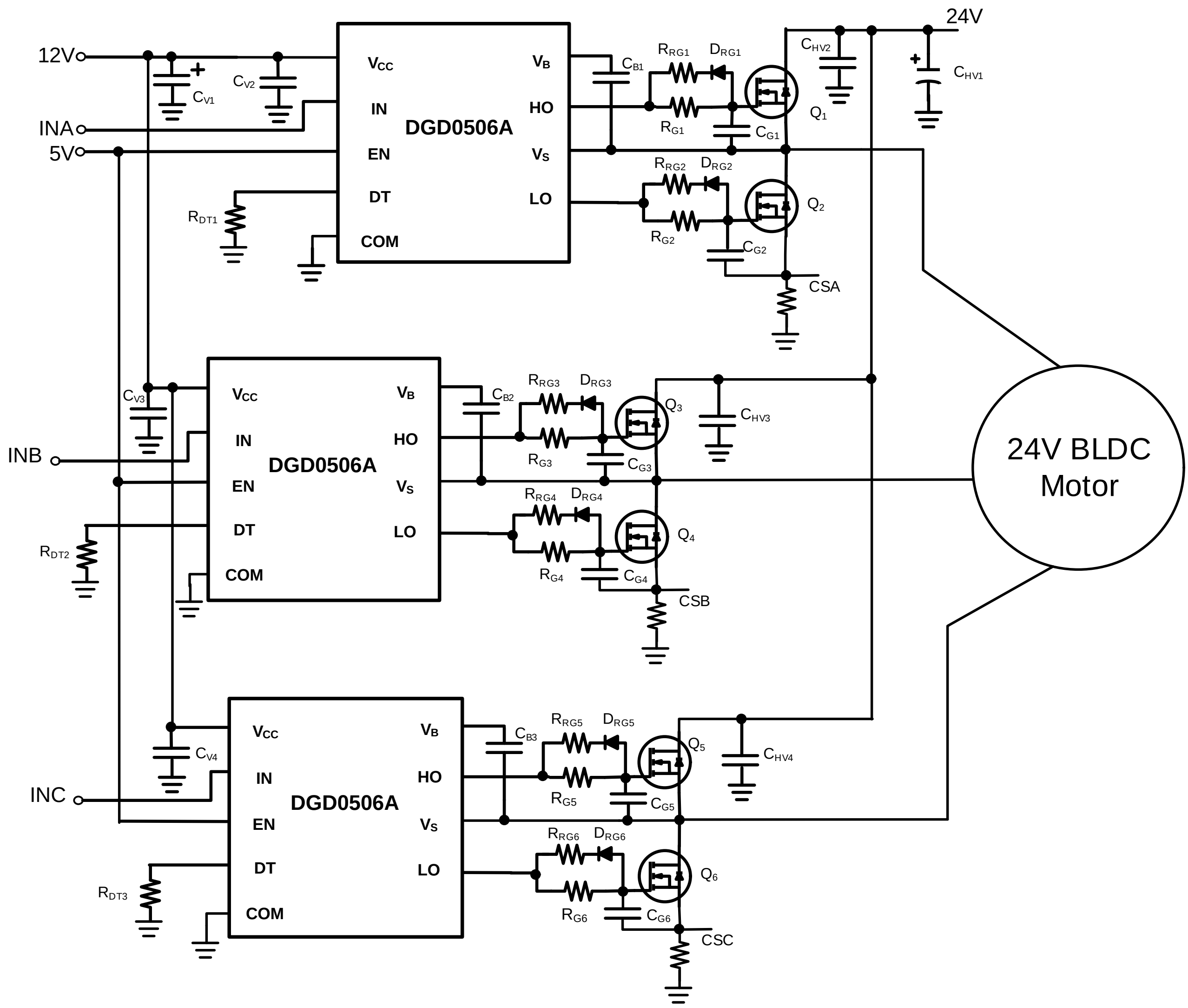

Figure 1. BLDC motor driver example application using the DGD0506A

Bootstrap Component Selection

Considering Figure 1, when the Low-side MOSFET (Q2, Q4 or Q6) turns on, V_S pulls to GND and the bootstrap capacitor (C_{B1}, C_{B2}, or C_{B3}) is charged. When the High-side MOSFET (Q1, Q3, or Q5) is turned on, V_S swings above V_{CC} and the charge on the bootstrap capacitor (C_B) provides current to supply the IC High-side Gate Driver. The charge on C_B is provided by V_{CC} through the integrated bootstrap diode and bootstrap resistor, and often the first charge of C_B at power up will be the largest current through the bootstrap circuit as typically C_B is not fully discharged at each cycle during normal operation.

Bootstrap Capacitor Discussion

The initial step in determining the value of the bootstrap capacitor (C_B) is to determine the maximum voltage drop (ΔV_{BS}) that can be guaranteed when the High-side device is turned on. In other words, V_{BSmin} must be greater than the UVLO of the High-side circuit, specifically V_{BSUV-} level. Therefore, if V_{BSmin} is the minimum V_{BS} such that:

$V_{BSmin} > V_{BSUV-}$

Then:
$\Delta V_{BS} = V_{CC} - V_F - V_{BSmin} - V_X$

Where

- V_{CC} is the supply voltage to the DGD0506A
- V_F is the voltage drop across the internal bootstrap diode (D_{BS})
- V_X is the voltage drop across the MOSFET

V_X is calculated as the current seen across Low-side MOSFET multiplied by its $R_{DS(ON)}$.

In addition to the voltage drops across these components, other factors that cause V_{BS} to drop are leakages, charge required to turn on the power devices, and duration of the High-side on time. The total charge (Q_T) required by the Gate Driver then equals:

$Q_T = Q_G + Q_{LS} + [I_{LK\_N}] * T_{HON}$

Where
Q_G = gate charge of power device
Q_{LS} = level shift charge required per cycle
T_{HON} = High-side on time
I_{LK_N} = sum of all leakages that include:

- I_{GSS}/I_{GES}: Gate-source leakage of the power device
- I_{LK_DB}: Bootstrap diode leakage
- I_{LK_IC}: Offset supply leakage of HVIC
- I_{QBS}: Quiescent current for High-side supply
- I_{LK_CB}: Bootstrap capacitor leakage

Bootstrap capacitor leakage (I_{LK_CBS}) only applies to electrolytic types. Therefore, it is best not to use electrolytic capacitor. Thus, bootstrap capacitor leakages will not be included in the calculations.

Q_{LS} is not listed in the datasheet; for the lower voltage process technology a Q_{LS} of 5nC will be a good approximation and provide a sufficient margin.

From the basic equation, then the minimum bootstrap capacitor is calculated as:

$C_{Bmin} \geq Q_T / \Delta V_{BS\_max}$

Example using MOSFET

The follow example uses a power MOSFET as the switching device with the following and desired parameters:

- Power device = DMN6017SK3
- Gate Driver = DGD0506A
- V_{CC} = 12V
- Q_G = 26nC
- I_{GSS} = 100nA
- T_{HON} = 5µs
- $R_{DS(ON)}$ = 25mΩ, 125°C
- I_{OUT} = 10A
- I_{QBS} = 100µA
- I_{LK_IC} = 50µA
- Q_{LS} = 5nC

- V_F = 1.0V
- I_{LK_DB} = 1µA
- V_{BSmin} = 3.3V

From equations above:

ΔV_{BS_max} = 12V- 1.0V-7.0V-0.25V = 7.45V

$Q_T = Q_G + Q_{LS} + [I_{LK\_N}]*T_{HON}$; where $I_{LK\_N} * T_{HON}$ = 0.75nC

Thus Q_T = 26nC + 5nC +0.75nC = 31.75nC

Therefore C_{Bmin} = 31.75nC / 7.45V= 4.26nF

The bootstrap capacitor calculated in the above problem is the minimal value required to supply the needed charge. It is recommended that a margin of 2-3 times the calculated value be used, minimally. Utilizing values lower than this could result in over charging of the bootstrap capacitor especially during $-V_S$ transients. Typically for high-speed applications like power supplies, C_B = 0.1µF to 1µF are used; and for low-speed applications like motor drives, C_{BS} = 1.0µF to 2.2µF are used. It is recommended to use low ESR ceramic capacitors as close to the V_B and V_S pin as possible (see PCB layout suggestions section).

Integrated Bootstrap Diode

The DGD05463/06A has an integrated bootstrap diode to minimize the system BOM and to ease system design. From a DC perspective, the data below from the datasheet shows the performance of the integrated bootstrap diode:

Forward Voltage of Bootstrap Diode	V_{F1}	—	0.67	—	V	I_F = 100µA
Forward Voltage of Bootstrap Diode	V_{F2}	—	1.7	—	V	I_F = 100mA

The current through the integrated bootstrap diode is typically the largest during the first charge of C_B. And the current waveform, as well as the time to charge C_B is determined by the size of the C_B, see below Figure 2 and Figure 3.

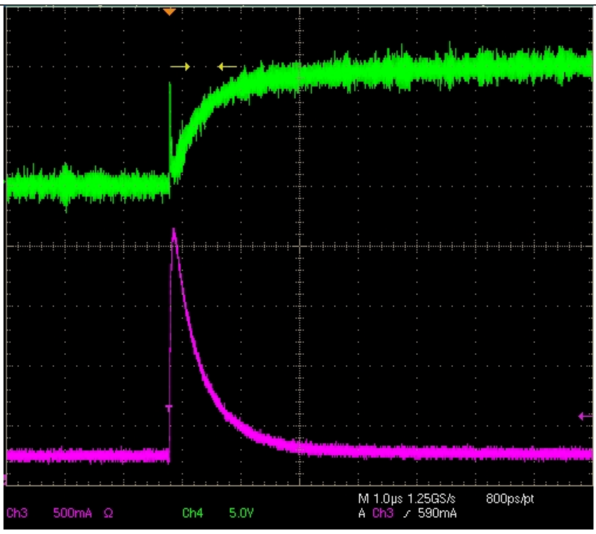

Figure 2. Bootstrap inrush current (Ch3) and V_{BS} (Ch4) with C_B = 0.1µF

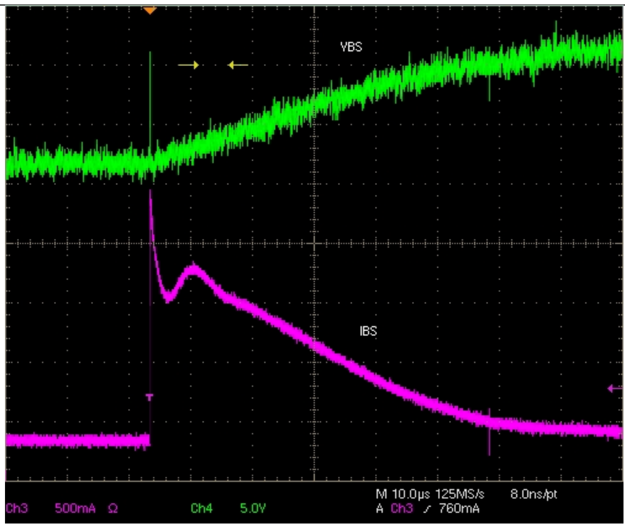

Figure 3. Bootstrap inrush current (Ch3) and V_{BS} (Ch4) with C_B = 10µF

Gate Component Selection

The most crucial time in the gate drive is the turn on and turn off of the MOSFET, and performing this function quickly, but with minimal noise and ringing is key. Too fast a rise/fall time can cause unnecessary ringing and poor EMI, and too slow a rise/fall time will increase switching losses in the MOSFET.

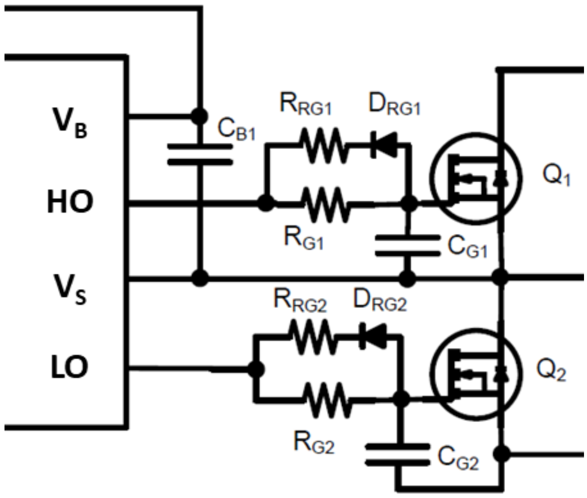

Figure 4. Gate drive High-side and low-side components for DGD0506A

Considering the Gate Driver components for DGD0506A in Figure 4, with the careful selection of R_{G1} and R_{RG1}, it is possible to selectively control the rise time and fall time of the gate drive to the MOSFET. For turn on, all current will go from the IC through R_{G1} and charge the MOSFET gate capacitance, hence increasing or decreasing R_{G1} will increase or decrease rise time in the application. With the addition of D_{RG1}, the fall time can be separately controlled as the turn off current flows from the MOSFET gate capacitance, through R_{RG1} and D_{RG1} to the driver in the IC to V_S for High-side and COM for Low-side . So, increasing or decreasing R_{RG1} will increase or decrease the fall time. Sometimes finer control is not needed and only R_{G1} and R_{G2} is used.

Increasing turn on and turn off has the effect of limiting ringing and noise due to parasitic inductances, hence with a noisy environment, it may be necessary to increase the gate resistors. Gate component selection is a compromise of faster rise time with more ringing, and a poorer EMI but better efficiency, contrasted with a slower rise time with better EMI, better noise performance but poorer efficiency. The exact value depends on the parameters of the application and system requirements. R_{G1} and R_{G2} values are typically between 10Ω and 50Ω, optimal value decided by MOSFET gate capacitance and drive current of Gate Driver. Gate resistor values are increased to decrease system noise, minimize ringing, and hence lower EMI. R_{RG1} and R_{RG2} values are typically between 5Ω and 20Ω, optimal value decided by MOSFET gate capacitance and drive current of Gate Driver. Also sink current gate resister values are increased to decrease system noise, minimize ringing, and hence lower EMI.

To have equal switching times for High-side and low-side , it is recommended that the Gate Driver components for high-side and low-side are mirrored. For example, $R_{RG1} = R_{RG2}$, $D_{RG1} = D_{GR2}$ and $R_{G1} = R_{G2}$.

The gate to source capacitors, C_{G1} and C_{G2}, are used to minimize unexpected shoot-through in the half-bridge and to improve system stability. The shoot-through can decrease efficiency or even damage the MOSFETs; this phenomenon is discussed further on page 9. If the Ciss of the MOSFET is small and there is instability in the system performance, then add C_{G1} and C_{G2} to improve stability. To begin, C_{G1}=C_{G2}=1nF should improve system performance.

VCC Decoupling Capacitors

For optimal operation, V_{CC} decoupling is crucial for all Gate Driver ICs. With poor decoupling, larger V_{CC} transients will occur at the IC when switching, and for greater and longer V_{CC} drop the IC can go into UVLO.

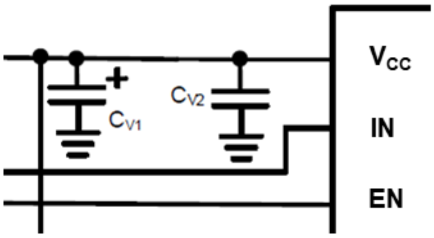

Figure 5. Suggested V_{CC} decoupling

As shown in Figure 5, two decoupling capacitors are recommended C_{V1} and C_{V2}. C_{V1} can be a larger electrolytic, for example 47µF, 50V, used to dampen low frequency drains on supply; C_{V1} does not need to be right next to the IC. But C_{V2} is used to decouple faster edge changes to V_{CC} and should be a low ESR ceramic capacitor placed close to the V_{CC} pin. This component provides stability when V_{CC} is quickly pulled down with load from the IC; typical values are 0.1µF to 1µF.

For applications with multiple Gate Driver ICs (For example the BLDC motor drive with 3 x Gate Drivers in Figure1), one larger electrolytic (C_{V1}) can be used and the three ceramic caps (C_{V2}, C_{V3}, C_{V4}) should be used close to the V_{CC} pin (see Layout section also).

High Voltage Decoupling Capacitors

Considering the performance of the whole Half-bridge, it is important to have appropriate high voltage decoupling capacitors (see C_{HV1}, C_{HV2}, C_{HV3}, and C_{HV4} in Figure 1). For best stability (best high frequency performance), C_{HV2}, C_{HV3}, and C_{HV4} are smaller ceramic capacitors (say 1µF 100V) placed close to the drain of the MOSFETs at the Half-bridge (less than 25mm); and then C_{HV1} is the electrolytic bulk capacitor which is typically part of the on-board power supply. If the small decoupling capacitors (C_{HV2}, C_{HV3}, and C_{HV4}) are not used, then for optimal operation, the bulk capacitor (C_{HV1}) should be close to the drain of the MOSFETs (less than 25mm). For even further high frequency decoupling, many parallel ceramic capacitors can be used; for example, 1.0µF in parallel with 3 x 0.1µF capacitors.

Input resistors

The IC PWM inputs, IN and EN, are very high impedance inputs with pull down resistors; The pull-down resistors on IN and EN have an approximate value of 200kΩ.

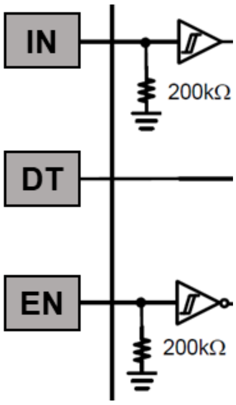

Figure 6. Input logic for the DGD05463/06A

Differences between DGD05463 and DGD0506A

The minimum allowed V_{CC} operating condition is the main difference between the DGD05463 and the DGD0506A. Hence the V_{CC} Recommended operating voltage and UVLO (both V_{CC} and V_{BS}) are the main specifications where the two devices differ.

Logic and Low-Side Fixed Supply Voltage	V_{CC}	4.5 (Note 9)	14	V
High-Side Floating Supply	V_B	V_S + 4.2	V_S + 14	V

Figure 7. Recommended operating voltages for the DGD05463

V_{CC} Supply Undervoltage Positive Going Threshold	V_{CCUV+}	3.3	3.8	4.2	V	—
V_{CC} Supply Undervoltage Negative Going Threshold	V_{CCUV-}	2.9	3.3	3.9	V	—

Figure 8. V_{CC} UVLO for the DGD05463 (V_{BS} UVLO is the same)

Logic and Low Side Fixed Supply Voltage	V_{CC}	8	14	V
High-Side Floating Supply	V_B	V_S + 8	V_S + 14	V

Figure 9. Recommended operating voltages for the DGD0506A

V_{CC} Supply Undervoltage Positive Going Threshold	V_{CCUV+}	6.0	7.0	8.0	V	—
V_{CC} Supply Undervoltage Negative Going Threshold	V_{CCUV-}	5.6	6.6	7.6	V	—

Figure 10. V_{CC} UVLO for the DGD0506A (V_{BS} UVLO is the same)

Suggestions for VCC = 5V operation using the DGD05463

Due to the performance of the Gate Driver outputs at low voltages, the minimal operating voltage level on V_B=4.3V. For V_{CC}=5V operation, this is not a concern for Low-side operation as it is operating at V_{CC}, but the high-side output driver is operating at a diode drop from internal bootstrap diode; hence when V_{CC}=5V, V_{BS}=4.3V, which would be ok. But for a system with operating V_{CC}=5V, it is typical to require V_{CC}=4.5V to 5.5V, and when V_{CC}=4.5V, VB will be below the recommended operating condition. Hence when wanting to use V_{CC}=4.5V to 4.9V operation it is required to use an external Schottky diode (see Figure 11).

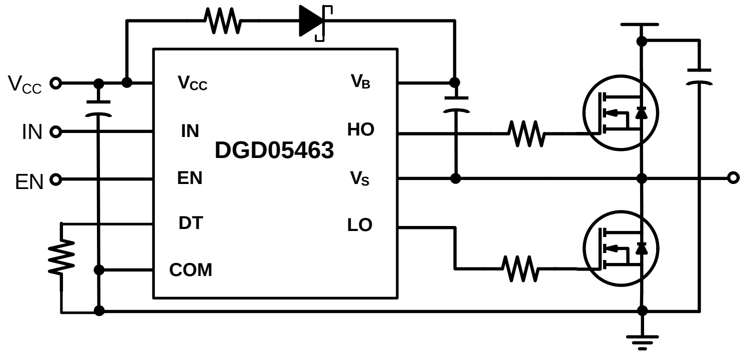

Figure 11. Typical application necessary for V_{CC}=4.5V to 4.9V, an external bootstrap Schottky will turn on before internal D_{BS}

Matching Gate Driver with MOSFET

IC drive current and MOSFET gate charge

Gate Driver ICs are defined by their output drive current, its ability to source current to the gate of the MOSFET at turn on and to sink current from the gate of the MOSFET at turn off. For the DGD05463 the drive current is IO+ = 1.5A typical and IO- = 2.5A typical.

For a given MOSFET, with the known drive current of the DGD05463, you can estimate how long it will take to turn on/off the MOSFET with the equation:
$t = Q_g / I$

Q_g = total charge of the MOSFET as provided by the datasheet
I = sink/source capability of the Gate Driver IC
t = calculated rise/fall time with the given charge and drive current

For example, with the Diodes' DMN6017SK3, 60V 43A, Q_g = 55nC; and with the DGD05463 IO+/IO, tr = 37ns and tf = 22ns. These are estimates as the total charge given in the datasheet may not be the same conditions in the application. An addition of a gate resistor will increase the tr and tf.

Unexpected shoot-through with dV_{DS}/dt

Unwanted MOSFET turn-on, caused by C_{GD} x dV_{DS}/dt (see Figure 12) is often the cause of unexplained shoot through in the Half-bridge circuit. Depending on the ratio of the C_{GS}/C_{GD}, when the dV_{DS}/dt across Low-side MOSFET (Q2) occurs (i.e when High-side MOSFET turns on), there can be a voltage applied to the gate of the Q2 MOSFET, turning on Q2 and causing shoot through. In effect a gate bouncing occurs causing a ringing on the V_S line and the power ground.

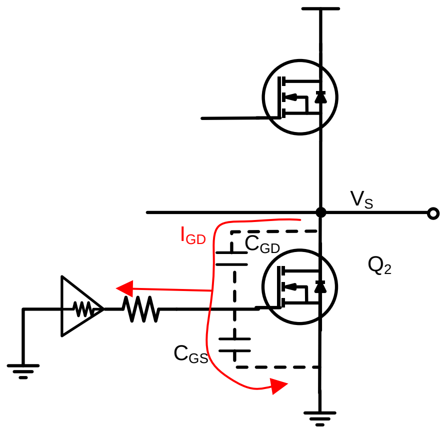

Figure 12. Unexpected shoot through with dV_{DS}/dt

Considering Figure 12

$I_{GD} = C_{GD} \times dV_{DS}/dt$

I_{GD} will flow towards the resistive load (and small inductive due to parasitics) of the Gate Driver and the C_{GS} of the MOSFET. Hence this unwanted condition may be minimized by looking at the Ciss/Cres in the MOSFET datasheet (Ciss/Cres gives an indication of C_{GS}/C_{GD}); having a Ciss/Cres as large as possible will minimize this phenomenon. An external capacitor can be added to the gate-source of the MOSFET (for example 1nF) which will increase C_{GS}/C_{GD}.

Minimum Pulse Operation

The DGD05463/06A has an RC filter on the input lines to be more resilient in noisy environments. During typical operation, the DGD05463/06A will respond to an input pulse greater than about 40ns. Hence for an input pulse greater than 40ns approximately, the IC will follow the pulse as expected; and for an input pulse less than 40ns, there will be no response from the IC.

PCB layout suggestions

Layout also plays a considerable role since unwanted noise coupling, unpredicted glitches and abnormal operation could arise due to poor layout of the associated components. Figure 13 shows the schematic with parasitic inductances in the high current path (L_{P1}, L_{P2}, L_{P3}, L_{P4}) which would be caused by inductance in the metal of the trace. Considering Figure 8, the length of the tracks in red should be minimized and the bootstrap capacitor (C_B) and the decoupling capacitor (C_D) should be placed as close to the IC as possible as well as using low EST ceramic capacitors. Finally, the gate resistors (R_{GH} and R_{GL}) and the sense resistor (R_S) should be surface mount devices. These suggestions will reduce the parasitics due to the PCB traces.

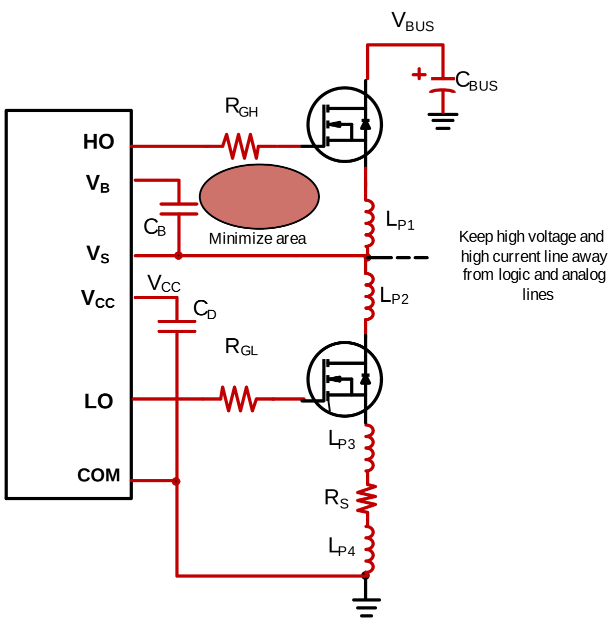

Figure 13. Layout suggestions for DGD05463/06A in a Half-bridge, lines in red should be as short as possible

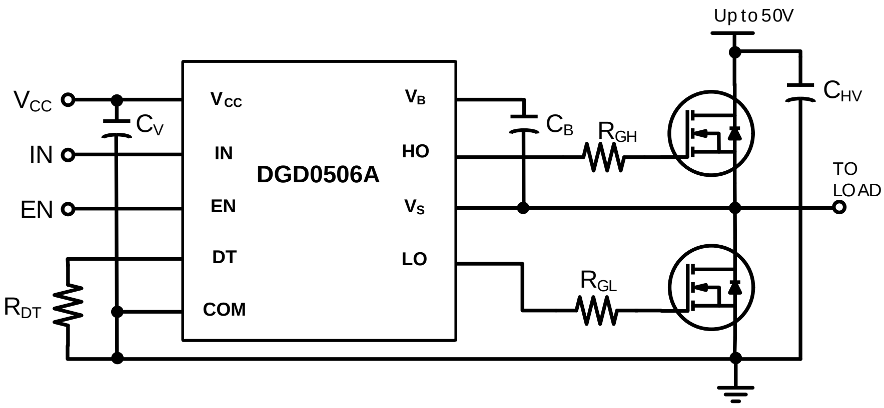

Figure 14. Schematic for layout example shown in Figure 15

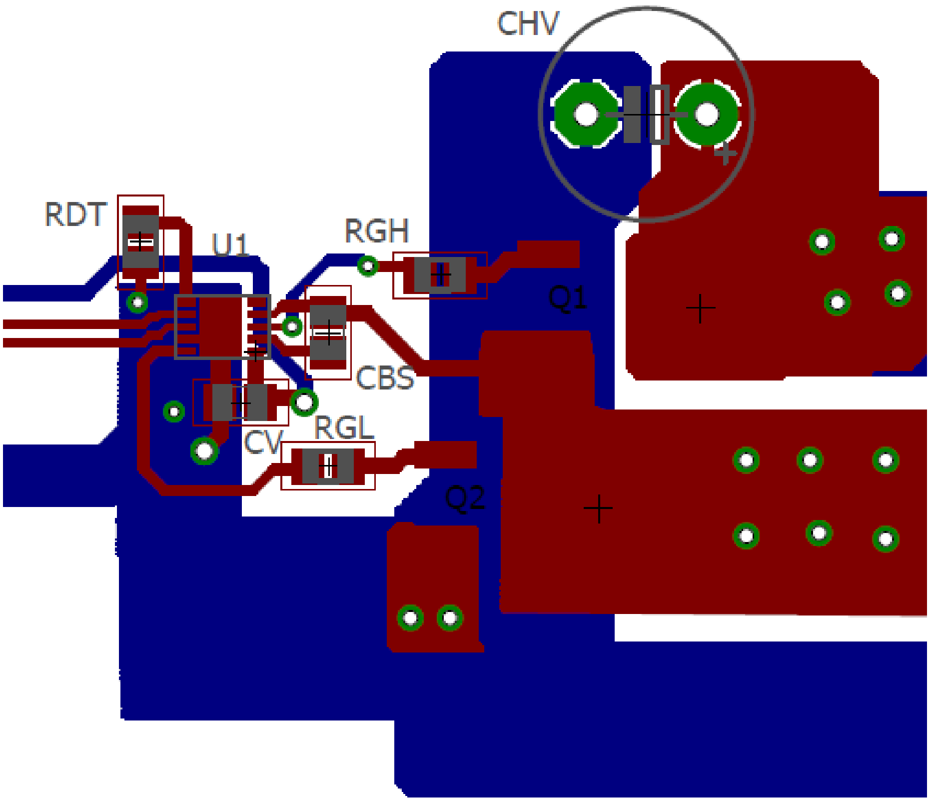

Figure 15. Suggested layout of the schematic shown in Figure 14, DGD0506A in DFN3030-10