User Guide for PI7C8148 Reference Board

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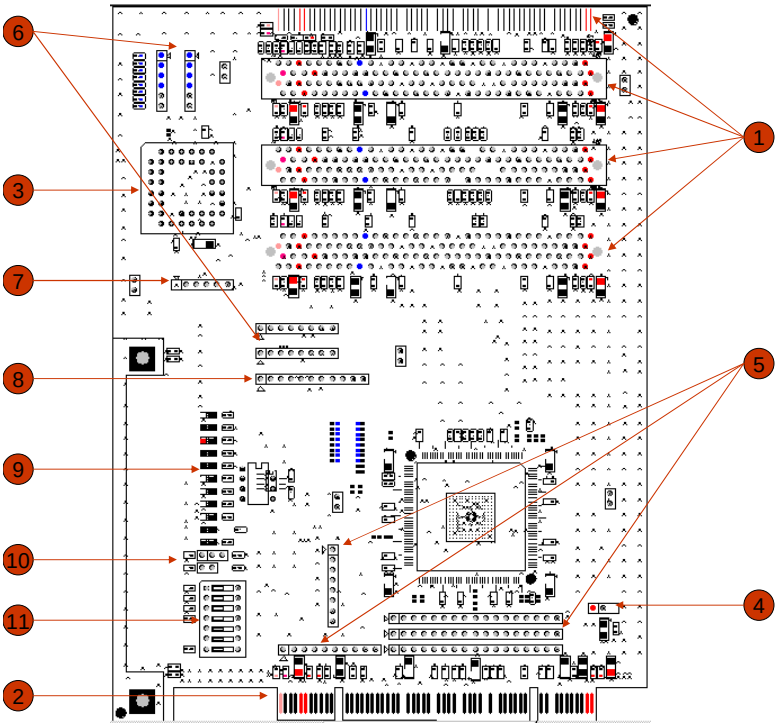
Introduction

The Pericom PI7C8148 PCI bridge evaluation board demonstrates the bridge and allows testing of key features either before or during design / layout stages. The PI7C8148 PCI Bridge complies with PCI Local Bus Specification Revision 2.2, PCI-to PCI Bridge Architecture Specification Revision 1.1 and PCI Power Management Interface Specification Revision 1.1.

Quick start (*photo of PI7C8148 reference board*)

The numbers on the photo correspond to the text explanation on the right:



1) 3 standards and one straddle mount PCI connector.
2) Pin 1 on the golden PCI edge connector faces left when looking down on the component (bridge IC).
3) External arbiter socket
4) Secondary bus Vio select : 3.3V or 5V
5) Primary bus test points
6) Secondary bus test points
7) JTAG connector
8) GPIO & Hot Swap test points
9) Power, GPIO & Hot Swap Led indicator
10) Hot Swap eject switch
11) Switches to set internal arbiter disable/enable, bus mode settings and some misc. functions

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This board comes **already configured** to support:

a) Secondary PCI voltage (S_VIO) is set to 3.3V.
b) Internal arbiter is enable
c) Hot Swap eject switch is pulled high.

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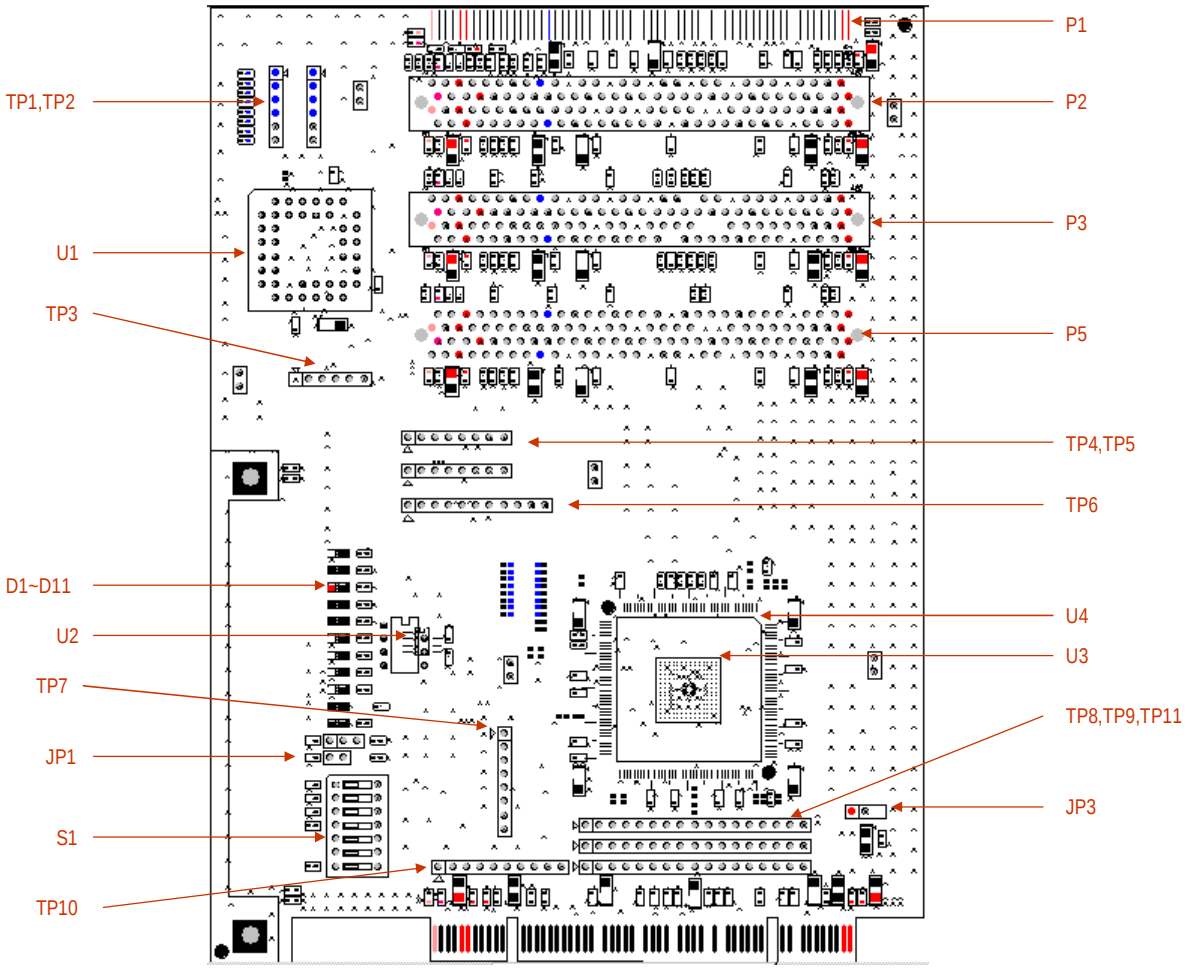
Components and Jumper Reference



U1	Socket for optional external arbiter
U2	Serial ROM for 8148 configuration
U3	Pericom PI7C8148 Bridge
U4	FPGA160 for testing usage
P1	Secondary bus slot 3
P2	Secondary bus slot 2
P3	Secondary bus slot 1
P5	Secondary bus slot 0
TP1, TP2 **TP4, TP5**	Secondary bus test points
TP3	JTAG connector
TP6	GPIO & Hot Swap test points
TP7~TP11	Primary bus test points
D1~D11	Power, GPIO & Hot Swap LED indicator
JP1	Hot Swap eject switch
JP3	SVIO 3.3V or 5V select
S1	Switches to set internal arbiter disable/enable, bus mode settings and some misc. functions

TABLES:

a) The right side of the board has a table of test points TP8, TP9 and TP11.

b) The component U1, U4 and TP3 is for special testing usage. And there is no any side effect for this unconnected part.

Please contact Pericom if you have any requirement for this issue.

Default Switch and Jumper Settings at a Glance

S1	Signal	Default	Description (ON: 'Low' or 'Connect', OFF: 'High' or 'Disconnect')
1	BPCCE	OFF	**'OFF'** - when PI7C8148 is under the D2 or D3 hot power state, the secondary bus will be placed at the B2 power state.
2	S_CFN#		For special testing usage
3	SCAN_TM#	OFF	**'OFF'** – for normal operation, scan chain disable
4	CTRL_S_M66EN	OFF	**'OFF'** – Put the secondary bus clock is under the 66Mhz
5	S_M66EN	OFF	**'OFF'** – Disconnect the S_M66EN with the **CTRL_S_M66EN** setting
6	EDGE_M66EN	OFF	**'OFF'** – Disconnect the S_M66EN with the primary bus *M66EN* setting
7	EDGE_PME#	OFF	**'OFF'** – Disconnect the S_PME# with the primary bus *PME#* setting

JP1 Eject switch is pulled high.
JP3 SVIO configured to 3.3V

Before Powering the Board

a) Seat the board into a PCI slot on the main system board.
Please look from the front of the motherboard, the small lip on our reference board points to the back of the motherboard, and the component side with the PI7C8148 bridge chip is on the left hand side.

b) Connect any PCI cards desired on the secondary PCI bus.
For all PCI connectors on our reference board, when looking down onto the PI7C8148 Bridge IC, pin 1 is on the left side of the board. This also applies to the top mounted "straddle" connector. Also each PCI connector has "A1", "B1", "A62", "B62" at the 4 corners of each slot, as a reminder where pin 1 is on each connector.

At this time, the Pericom PI7C8148 reference board is ready to use.

Primary Bus Test Points – TP8, TP9 and TP11:

For allowed a logic analyzer or oscilloscope to monitor signals on the path between the PI7C8140 and the primary bus. There are 3 rows of 17 pin connectors, labeled TP8, TP9 and TP10

	1	2	3	4	5	6	7	8	9
TP8	GNT#	AD30	AD27	AD24	AD22	AD19	AD16	IRDY#	STOP#
TP9	REQ#	AD29	AD26	CBE3#	AD21	AD18	CBE2#	TRDY#	LOCK#
TP11	AD31	AD28	AD25	AD23	AD20	AD17	FRAME#	DEVSEL	PERR#
	10	11	12	13	14	15	16	17	
TP8	SERR#	AD15	AD12	AD9	AD7	AD3	AD1	GND	
TP9	PAR	AD14	AD11	CBE0#	AD6	AD5	AD0	GND	
TP11	CBE1#	AD13	AD10	AD8	AD4	AD2	IDSEL	GND	

Test Points Description:

For allowed convenient sampling of signals by logic analyzer or oscilloscope:

TP1,

	1	2	3	4	5	6
TP1	SLOT_REQ2#	SLOT_GNT2#	SLOT_REQ3#	SLOT_GNT3#	GND	GND

TP2,

	1	2	3	4	5	6
TP2	SLOT_REQ0#	SLOT_GNT0#	SLOT_REQ1#	SLOT_GNT1#	GND	GND

TP3,

	1	2	3	4	5	6
TP3	VCC	TCK	TDI	TDO	TMS	GND

TP4,

	1	2	3	4	5	6	7	8
TP4	S_IDSEL3	S_IDSEL2	S_IDSEL1	S_IDSEL0	P_CLKRUN#	S_CLKRUN#	GND	GND

TP5,

	1	2	3	4	5	6	7	8
TP5	S_RST#	S_CLKOUT3	S_CLKOUT2	S_CLKOUT1	S_CLKOUT0	GND	GND	GND

TP6,

	1	2	3	4	5	6
TP6	GPIO3	GPIO2	GPIO1	GPIO0	EEPCLK	EEPD
	7	8	9	10	11	
TP6	ENUM#	EJECT	L_STAT	GND	GND	

TP7,

	1	2	3	4	5	6
TP7	BPCCE	S_CFN#	SCAN_TM#	SCAN_EN	S_M66EN	S_PME#
	7	8				
TP7	GND	GND				

TP10,

	1	2	3	4	5	6
TP10	EDGE_INTA#	EDGE_INTB#	EDGE_INTC#	EDGE_INTD#	EDGE_PME#	EDGE_M66EN
	7	8	9	10		
TP10	P_RST#	P_CLK	GND	GND		

Special Concerns

Due to test purpose, the 8148 reference board leaves some part for specific experiment. And these unconnected parts can not impact the system any more. Please contact with the Pericom if you need any help for this issue.

Please reference the following unconnected part list:

1) C100
2) CT1~CT17
3) JP2
4) RNS1~RNS11
5) R76, R85
6) TP3
7) U1, U4